

**1.0**

**SHEET**

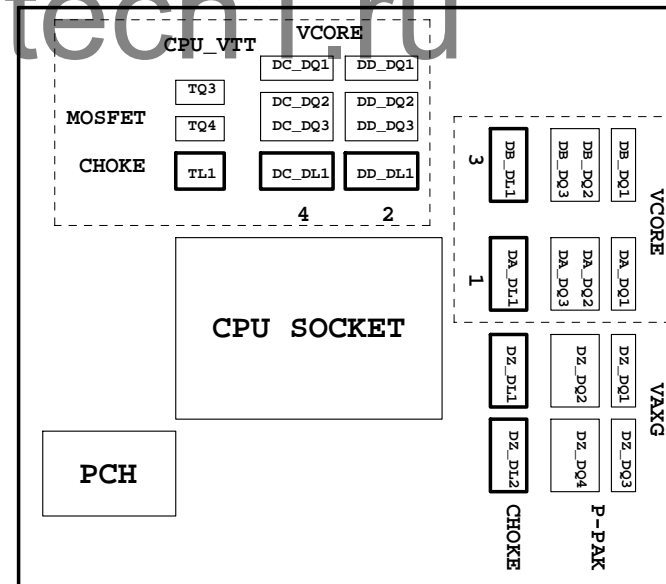
**TITLE**

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX1*3 , PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1&2
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS , TPM SLB9635TT
21	VT2021 CODEC
22	REAR AUDIO JACK
23	VCORE PWM_IR3564
24	VCORE PWM DRIVER IR3598
25	NCP3933 OVER VOLTAGE
26	DISCRETE POWER
27	DDR 15V & CPU VTT PWM IR3570

**SHEET**

**TITLE**

28	DDR_15V & CPU_VTT PWM DRIVER CHL8550
29	VCCSA POWER
30	F_PANEL , F_USB2.0/3.0
31	ATX POWER, CLOCK GEN
32	HWM , KB/MS , FAN CTRL
33	LAN ATHEROS AR8151
34	N/A
35	M-SATA
36	DVI
37	HDMI , R_USB30
38	TABLE LIST
39	
40	



**Gigabyte Technology**

**Cover Sheet**

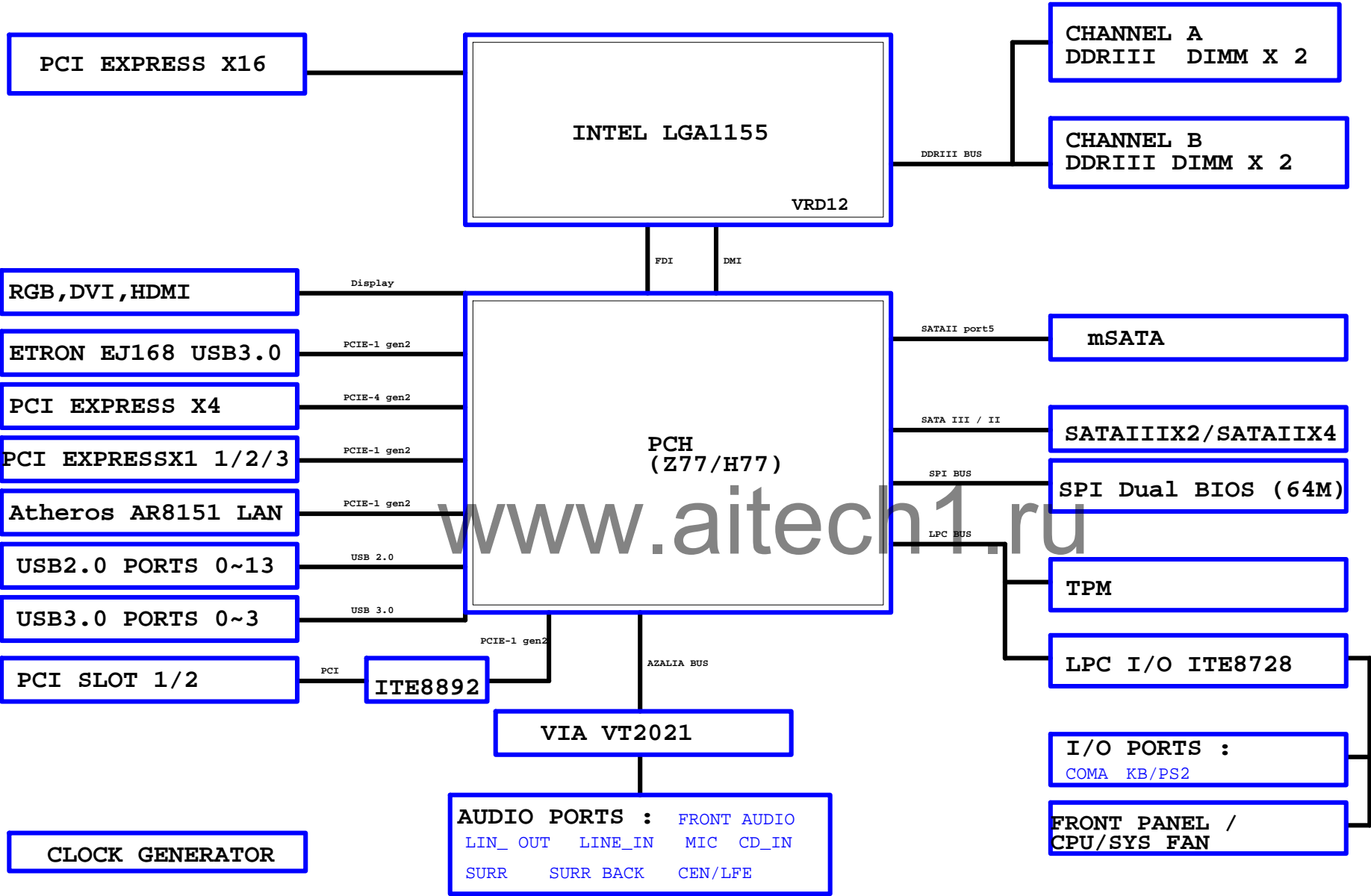
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Cover Sheet			
Size Custom	Document Number	GA-Z77-D3H	Rev 1.0
Date:	Monday, January 09, 2012	Sheet 1 of 38	

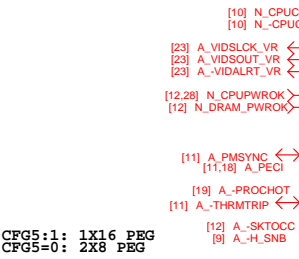
## Component value change history

[illegible]

DATE	Change Item	Reason
P67X-UD3-B3		
2011/02/18-0.1	1. 移除LAR11 ,LAR14 , NR28 ,新增NTP11	
2011/02/18-1.0	2. 新增DR388,DR389,DR391 ; Remove DQ49,DR347,DR371 3. CR44改成R0603-RH 4. R1,LAR3,RBR20,LABC25 -->R0402-2-SHORT 5. RAQ1 --> Q_TO223-MASK 6. RARN1 --> R8P4R-0402-SHORT 7. CESD1-5 --> SSOP5 8. RAQ2,RAEC1一起往下移40mil 9. CESD2文字面要標pin1	
2011/03/8-1.01	1. Add "Dolby" logo	
2011/03/8-1.02	1. UAFB1,UAFB2,UBF1,UBF2 Footprint update 1206-->1812 2. Add "AD1" FOR 5VSB	
Z68XP-D3		
1.0	1. update MINI_PCIE footprint 2. 文字面 : SLOT部分全對齊	
Z77-D3H-0.1	EVT	
0.2-1216	1. Remove SE9172 ■ Add VCC3 內層(注意其他內層power,跨切割) 2. SPDIF AGND --> GND 3. PCI SLOT & PCIEX1/X4 CAP COST DOWN 4. 0 ohm --> SHORT PAD 5. REMOVE SMBUS FROM COMP TO SOLDER SIDE IN DR POWER 6. SATA3 connect Change to 90 degree (記得SATA3訊號部分要做挖空) 7. Add "108dB"文字面 8. Remove VCC1_05_PCH & VCC1_8_PCH gate net 9. Add EJ168 R_USB30_1 & F_USB3 10. UAE1/UAE2 NET SWAP 11. 內層+12V要打VIA在COMA處 12. SPDIFO_HDMI走12mil	
1.0	1. +12V內層加寬,0 ohm short排組留一個 2. SATA2-SATA3文字面要隱藏 3. NEC2/UAE3往右移,遠離PCH_HS 4. DART2 移至 DC_DQ1左上方 5. Q7 & DAR31 NET Change	
1.1	1. DDR_15V & CPU_VTT 補償改成487ohm+3.3nF	

BLOCK DIAGRAM

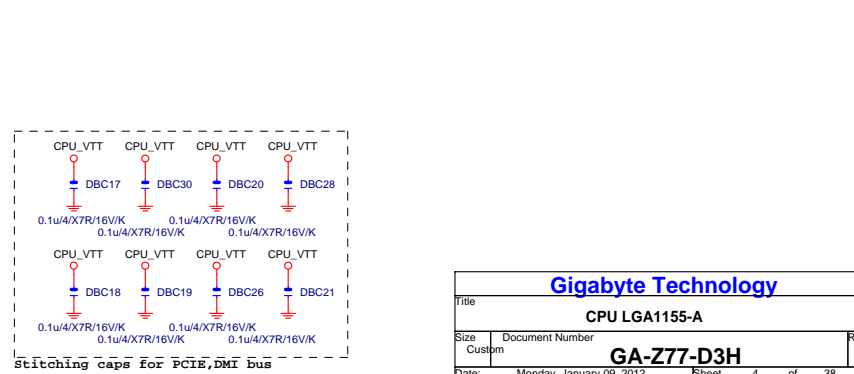
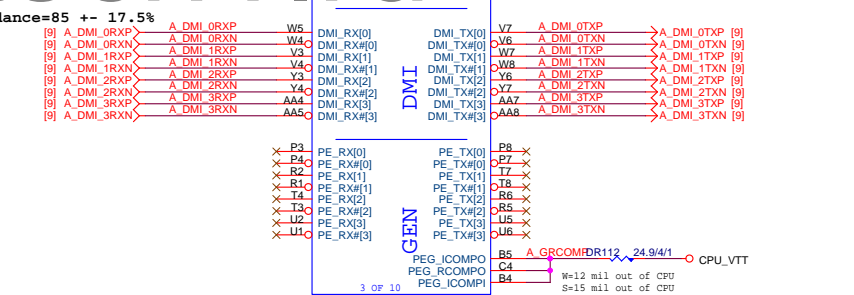
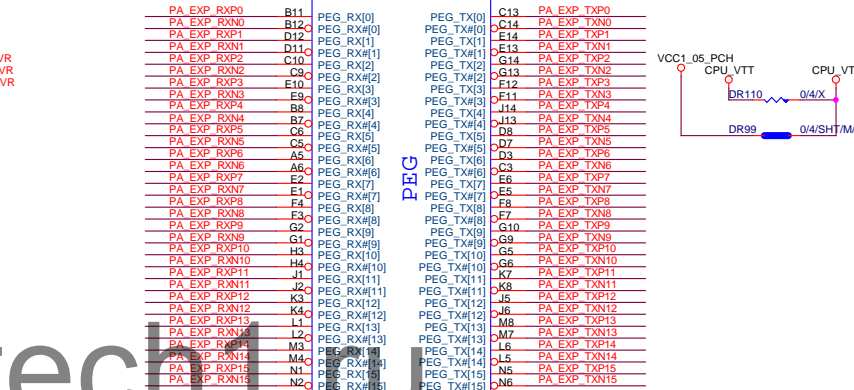
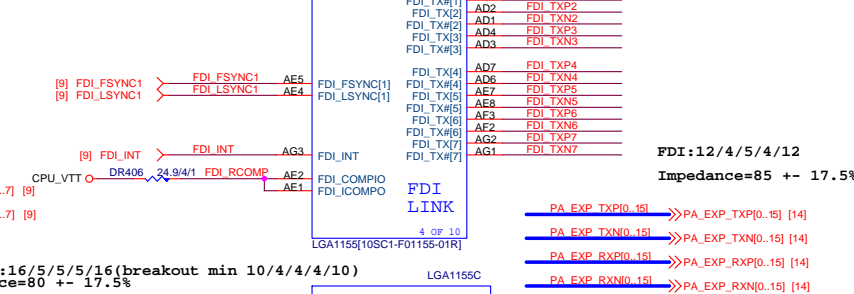
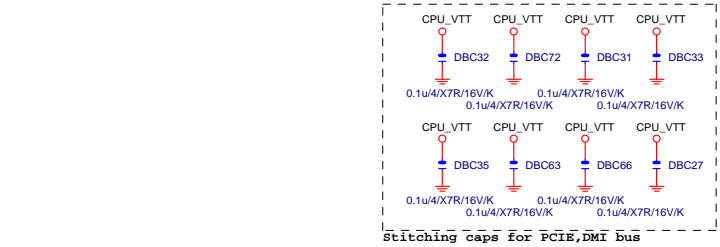
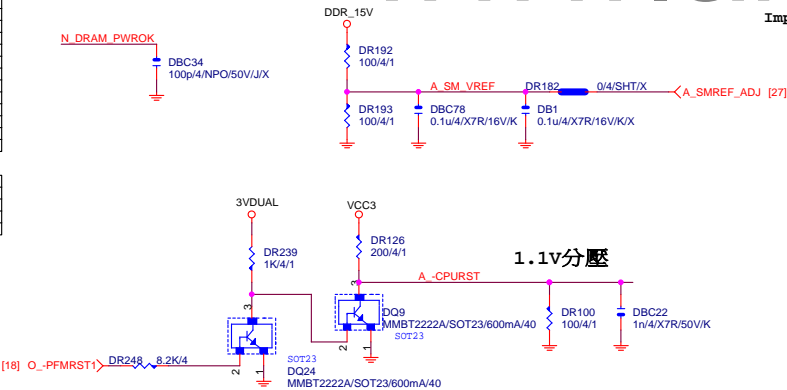




CFG	H	L	NOTE
0	RSVD	RSVD	RSVD
1	RSVD	RSVD	RSVD
2	Reverse	Reverse	LAIB REVERSAL[0],x16
3	RSVD	RSVD	RSVD
4	RSVD	RSVD	RSVD
7	RSVD	RSVD	RSVD
8	RSVD	RSVD	RSVD
9	RSVD	RSVD	RSVD
10	RSVD	RSVD	RSVD
11	RSVD	RSVD	RSVD
12	RSVD	RSVD	RSVD
13	RSVD	RSVD	RSVD
14	RSVD	RSVD	RSVD
15	RSVD	RSVD	RSVD
16	RSVD	RSVD	RSVD
17	RSVD	RSVD	RSVD

CFG6	CFG5	PCIE CONFIG
1	1	1X16, Default
1	0	2X8
0	1	RSVD
0	0	X8,X4,X4

CFG 0-17 all internal PULL-UP



LGA1155A		
M_AAA0	AV27	SA_MA[0]
M_AAA1	AY24	SA_MA[1]
M_AAA2	AW24	SA_MA[2]
M_AAA3	AW23	SA_MA[3]
M_AAA4	AV23	SA_MA[4]
M_AAA5	AT24	SA_MA[5]
M_AAA6	AT23	SA_MA[6]
M_AAA7	AU22	SA_MA[7]
M_AAA8	AV22	SA_MA[8]
M_AAA9	AT22	SA_MA[9]
M_AAA10	AV28	SA_MA[10]
M_AAA11	AU21	SA_MA[11]
M_AAA12	AT21	SA_MA[12]
M_AAA13	AW32	SA_MA[13]
M_AAA14	AU20	SA_MA[14]
M_AAA15	AT20	SA_MA[15]
[7] M_SWEA	M_SCASA	AV29
[7] M_SCASA	M_SRASA	AV30
[7] M_SBA0	M_SBA1	AW28
[7] M_SBA1	M_SBA2	AV20
[7] M-CSA0	M-CSA1	AV32
[7] M-CSA1	M-CSA2	AW30
[7] M-CSA2	M-CSA3	AU33
[7] M-CKEA0	M-CKEA1	AT19
[7] M-CKEA1	M-CKEA2	AU18
[7] M-CKEA2	M-CKEA3	AV18
[7] M_ODT_A0	AU31	SA_ODT[0]
[7] M_ODT_A1	AU32	SA_ODT[1]
[7] M_ODT_A2	AU30	SA_ODT[2]
[7] M_ODT_A3	AW33	SA_ODT[3]
[7] M-DCLKA0	M-DCLKA0	AY25
[7] M-DCLKA0	M-DCLKA1	AU24
[7] M-DCLKA1	M-DCLKA2	AW27
[7] M-DCLKA2	M-DCLKA3	AW26
[7] M-DCLKA3	M-DCLKA3	AW26
[7,8] M_DDR3_RST	AW18	SM_DRAMRST#
MBC8	0.1u4/X7R/16V/K/X	
AV13	SA_DQS[8]	
AV12	SA_DQS[8]	
AU12	SA_ECC_CB[0]	
AU14	SA_ECC_CB[1]	
AU13	SA_ECC_CB[2]	
AU13	SA_ECC_CB[3]	
AU11	SA_ECC_CB[4]	
AU12	SA_ECC_CB[5]	
AW12	SA_ECC_CB[7]	
AK3	M_DQSA0	
AK2	M_DQSA0	
AJ3	M_DA0	
AJ4	M_DA1	
AL3	M_DA2	
AL4	M_DA3	
AJ1	M_DA5	
AL2	M_DA6	
AL1	M_DA7	
AP3	M_DQSA1	
AP2	M_DQSA1	
AN1	M_DA8	
AN4	M_DA9	
AR3	M_DA10	
AR4	M_DA12	
AN2	M_DA13	
AR2	M_DA14	
AR1	M_DA15	
AW4	M_DQSA2	
AW4	M_DQSA2	
AV2	M_DA16	
AW3	M_DA17	
AV5	M_DA18	
AW5	M_DA19	
AU2	M_DA20	
AU3	M_DA21	
AU5	M_DA22	
AY5	M_DA23	
AV8	M_DQSA3	
AW8	M_DQSA3	
AY7	M_DA24	
AU7	M_DA25	
AW9	M_DA26	
AW7	M_DA29	
AW9	M_DA30	
AY9	M_DA31	
AV37	M_DQSA4	
AV36	M_DQSA4	
AU35	M_DA32	
AW37	M_DA33	
AU39	M_DA34	
AU36	M_DA35	
AW35	M_DA36	
AY36	M_DA37	
AU38	M_DA38	
AU37	M_DA39	
AP38	M_DQSA5	
AP39	M_DQSA5	
AR40	M_DA40	
AR37	M_DA41	
AN38	M_DA42	
AN37	M_DA43	
AR39	M_DA44	
AR38	M_DA45	
AN39	M_DA46	
AN40	M_DA47	
AK38	M_DQSA6	
AK39	M_DQSA6	
AL40	M_DA48	
AL37	M_DA49	
AJ38	M_DA50	
AJ37	M_DA51	
AL39	M_DA52	
AL38	M_DA53	
AJ39	M_DA54	
AJ40	M_DA55	
AF38	M_DQSA7	
AF39	M_DQSA7	
AG40	M_DA56	
AG37	M_DA57	
AE38	M_DA58	
AE37	M_DA59	
AG39	M_DA60	
AG38	M_DA61	
AE39	M_DA62	
AE40	M_DA63	

DDR\_0

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LGA1155[10SC1-F01155-01R]

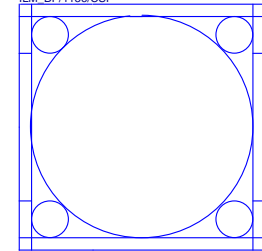
LGA1155B		
M_AAB0	AK24	SB_MA[0]
M_AAB1	AM20	SB_MA[1]
M_AAB2	AM19	SB_MA[2]
M_AAB3	AK18	SB_MA[3]
M_AAB4	AP19	SB_MA[4]
M_AAB5	AP18	SB_MA[5]
M_AAB6	AM18	SB_MA[6]
M_AAB7	AL18	SB_MA[7]
M_AAB8	AY17	SB_MA[8]
M_AAB9	AN18	SB_MA[9]
M_AAB10	AN23	SB_MA[10]
M_AAB11	AU17	SB_MA[11]
M_AAB12	AR26	SB_MA[12]
M_AAB13	AR26	SB_MA[13]
M_AAB14	AY16	SB_MA[14]
M_AAB15	AV16	SB_MA[15]
[8] M_SWEB	M_SCASB	AK25
[8] M_SCASB	M_SRASB	AP24
[8] M_SBA0	M_SBA1	AP23
[8] M_SBA1	M_SBA2	AW17
[8] M-CSB0	M-CSB1	AN25
[8] M-CSB1	M-CSB2	AN26
[8] M-CSB2	M-CSB3	AT26
[8] M-CKEB0	M-CKEB1	AY15
[8] M-CKEB1	M-CKEB2	AW15
[8] M-CKEB2	M-CKEB3	AV15
[8] M_ODT_B0	AL26	
[8] M_ODT_B1	AP26	
[8] M_ODT_B2	AM26	
[8] M_ODT_B3	AK26	
[8] M-DCLKB0	M-DCLKB0	AL21
[8] M-DCLKB0	M-DCLKB1	AL22
[8] M-DCLKB1	M-DCLKB2	AK20
[8] M-DCLKB2	M-DCLKB3	AP21
[8] M-DCLKB3	M-DCLKB3	AN21
[8] M_VREF_D0B	AH1	FC_AH1
[7] M_VREF_D0B	AH4	FC_AH4
AN16	SB_DQS[8]	
AN15	SB_DQS[8]	
AL16	SB_ECC_CB[0]	
AM16	SB_ECC_CB[1]	
AP16	SB_ECC_CB[2]	
AR16	SB_ECC_CB[3]	
AL15	SB_ECC_CB[4]	
AR15	SB_ECC_CB[5]	
AP15	SB_ECC_CB[7]	
AP32	M_DB40	
AP21	M_DB41	
AP35	M_DB42	
AP34	M_DB43	
AR32	M_DB44	
AR31	M_DB45	
AR35	M_DB46	
AR34	M_DB47	
AL33	M_DQSB6	
AM33	M_DQSB6	
AM32	M_DB48	
AM31	M_DB49	
AL35	M_DB50	
AL32	M_DB51	
AM34	M_DB52	
AL31	M_DB53	
AM35	M_DB54	
AL34	M_DB55	
AG35	M_DQSB7	
AG34	M_DQSB7	
AH35	M_DB56	
AH34	M_DB57	
AE34	M_DB58	
AE35	M_DB59	
AJ35	M_DB60	
AJ34	M_DB61	
AE33	M_DB62	
AF33	M_DB63	

DDR\_1

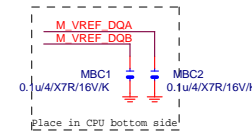
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LGA1155[10SC1-F01155-01R]

LGA1155  
ILM BP/1156/CSP



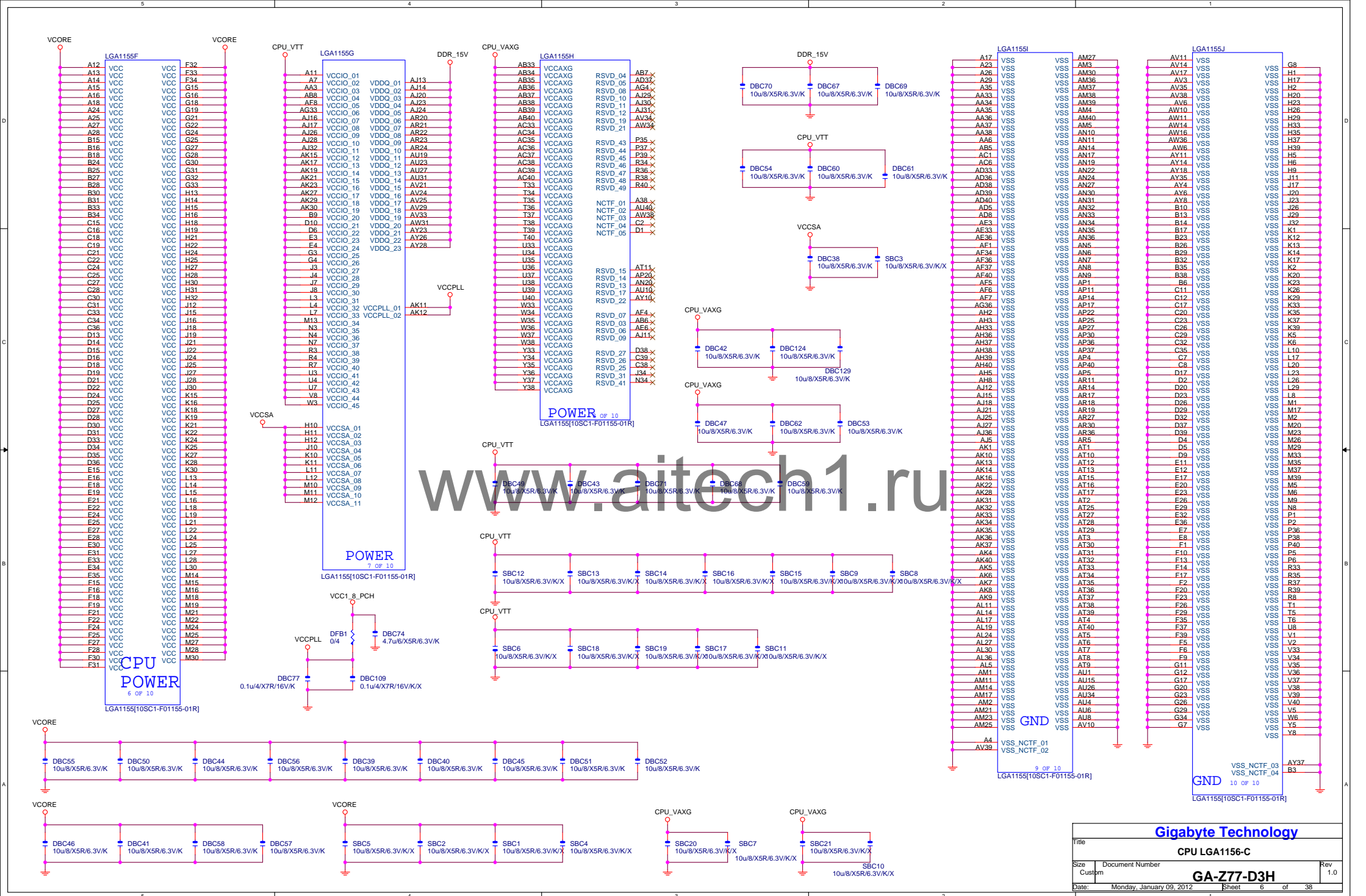
Need check the new CPU ME



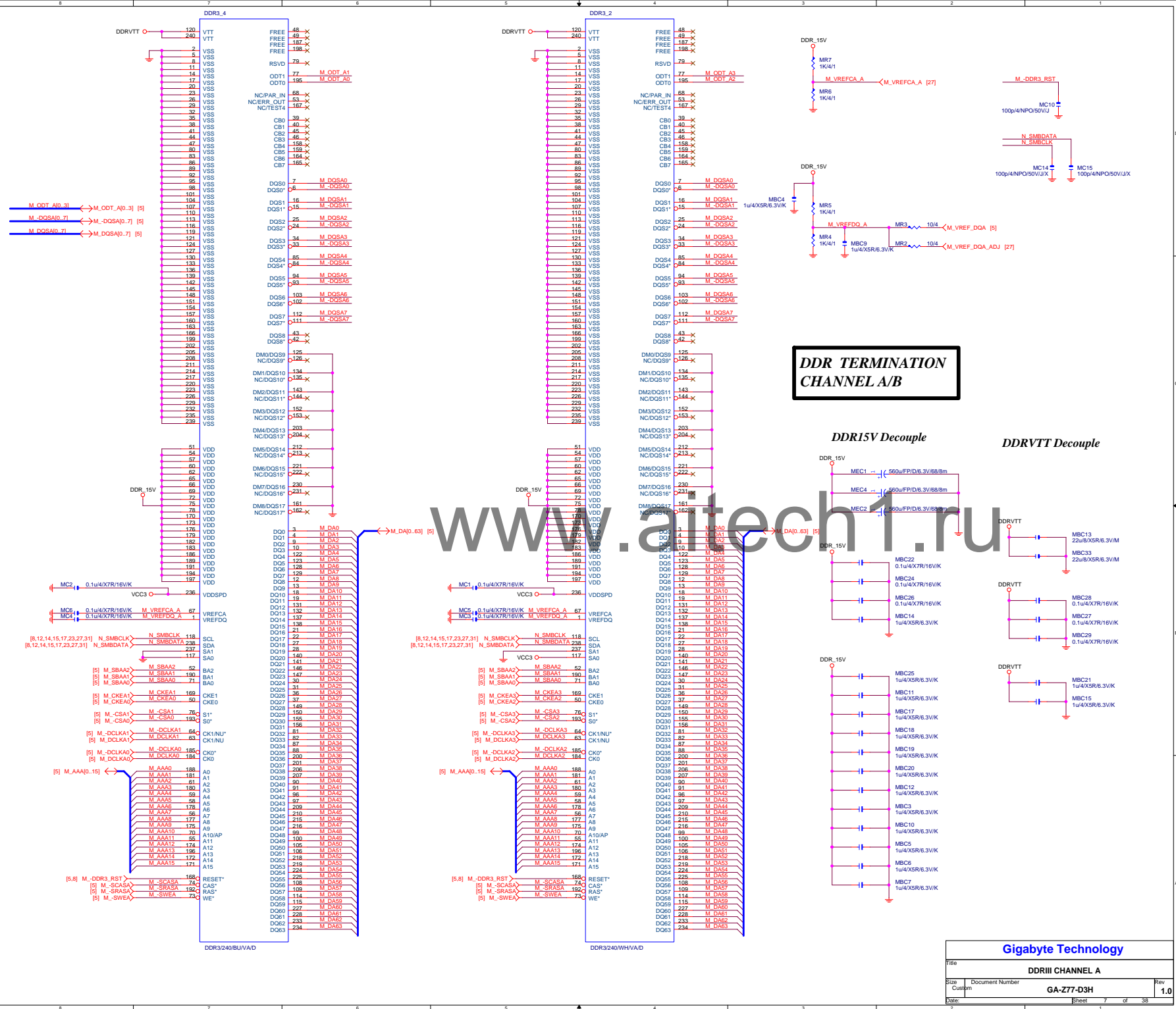
Gigabyte Technology

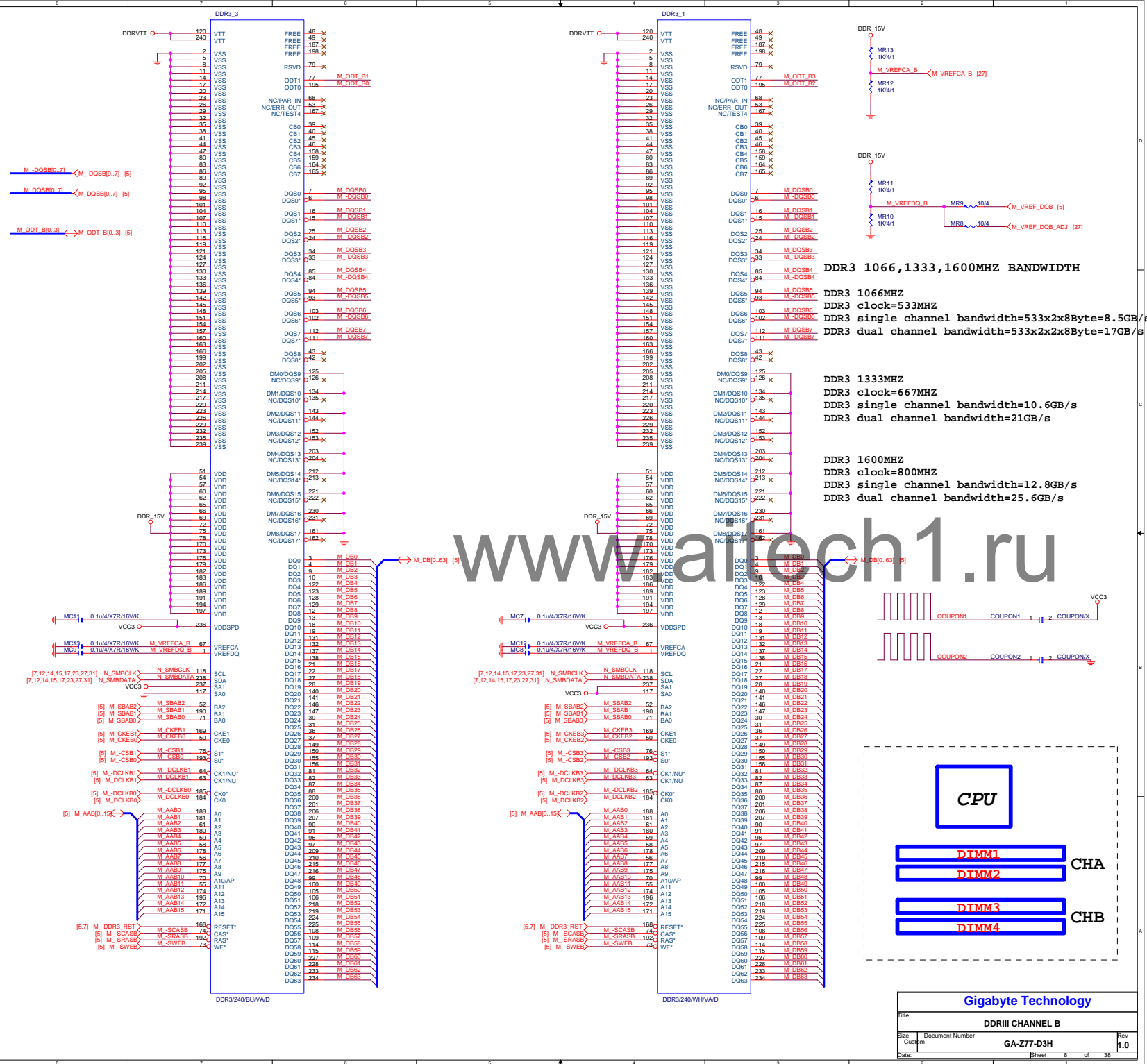
CPU LGA1156-B

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USB3.0:20/5/7/5/20 (breakout min 8/4/4/4/8) ; ONLY 3 VIAS  
Impedance=85 +- 17.5%  
Back Panel < 10000 MILS  
Front Panel < 6000 MILS

USB2.0 : 12/4.5/7.5/4.5/12 (breakout min 8/4/4/4/8)  
Impedance=90 +- 17.5%

PCBH

PCHG

FDILINK

BD82Z77/S

FDI:12/4/5/4/12  
Impedance=85 +- 17.5%

FDI\_TXP0\_7I >>> FDI\_TXP0[0..7] [4]  
FDI\_TXN0\_7I >>> FDI\_TXN0[0..7] [4]

PCHE

NVRAM

BD82Z77/S

USB OC#	Configure
OC0#	USB0_1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5#	USB10,11
OC6#	USB12,13
OC7#	Not Use

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放靠近 Device & PCI-E Slot

PCIEX1:16/5/5/5/16 (breakout min 8/4/4/4/8)

Impedance=80 +- 17.5%

VCC3  
NBC51  
1u4/X5R/6.3V/K

N-USBOC\_F  
NBC45  
0.1u4/X7R/16V/K

N-USBOC\_R  
NBC46  
0.1u4/X7R/16V/K

3VDUAL  
NR98  
8.2K/4

PCH\_HS

VCC1\_8\_PCH

NR118  
2.2K/4/1

NR117 4.7K/4 N NV CLE

A-H\_SNB [4]  
DMT / FDI termination voltage

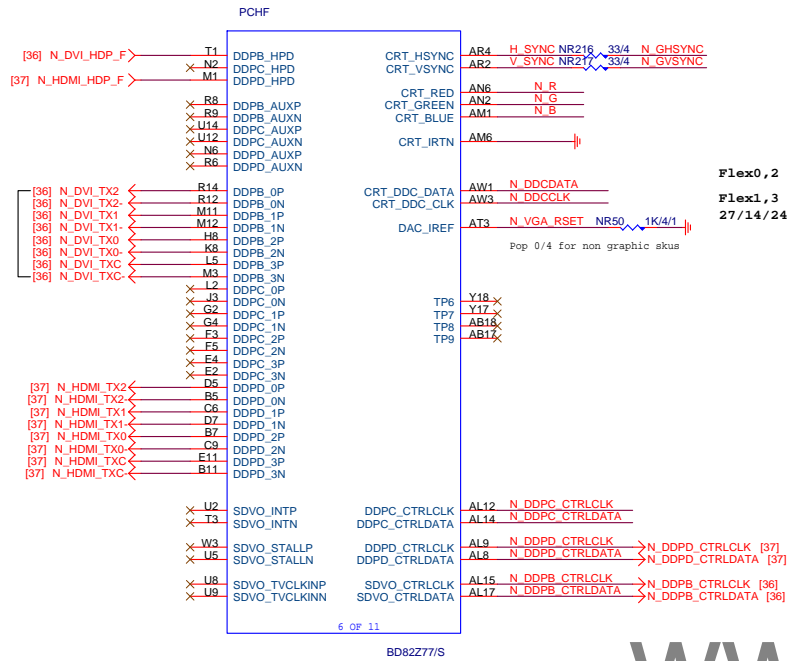
NBC57  
0.1u4/X7R/16V/K

Mount for integrated clock Generation Mode

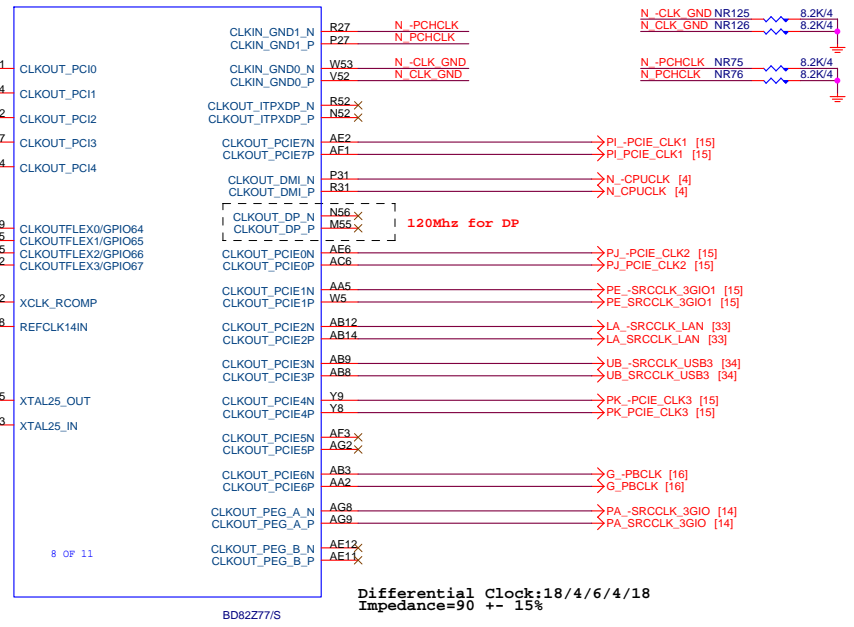
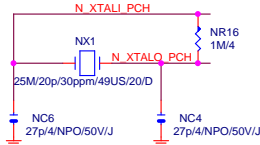
CK\_DOTCLK NR84 8.2K/4  
CK\_DOTCLK NR88 8.2K/4  
R102 short to GND in non graphic SKU

Gigabyte Technology

Title		
PCH FDI,DMI,USB,PCI-E		
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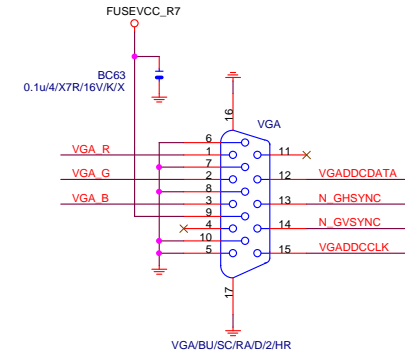
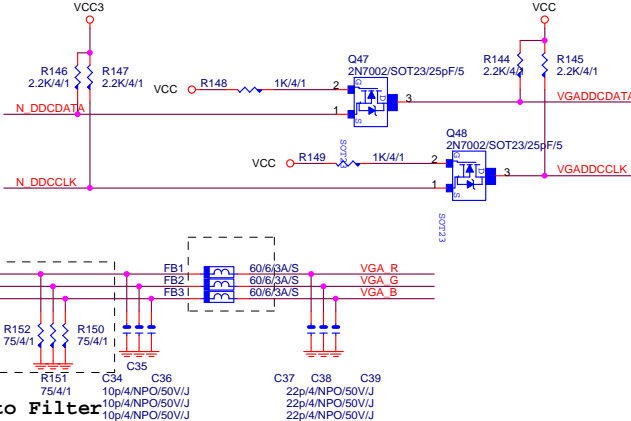
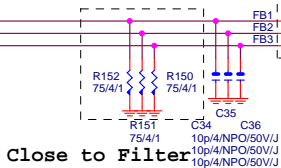
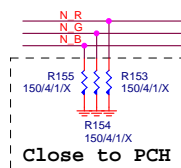
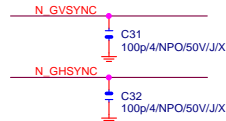
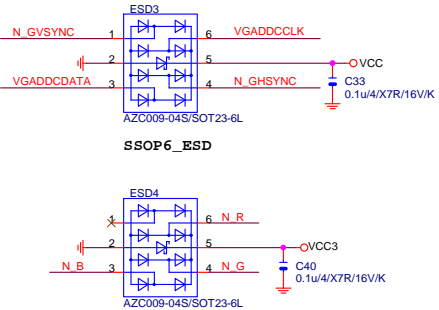
Flex0,2 : 33MHZ  
Flex1,3 :  
27/14/24/48/25MHZ



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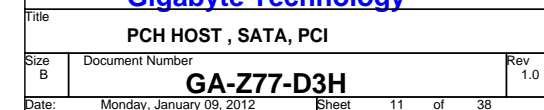


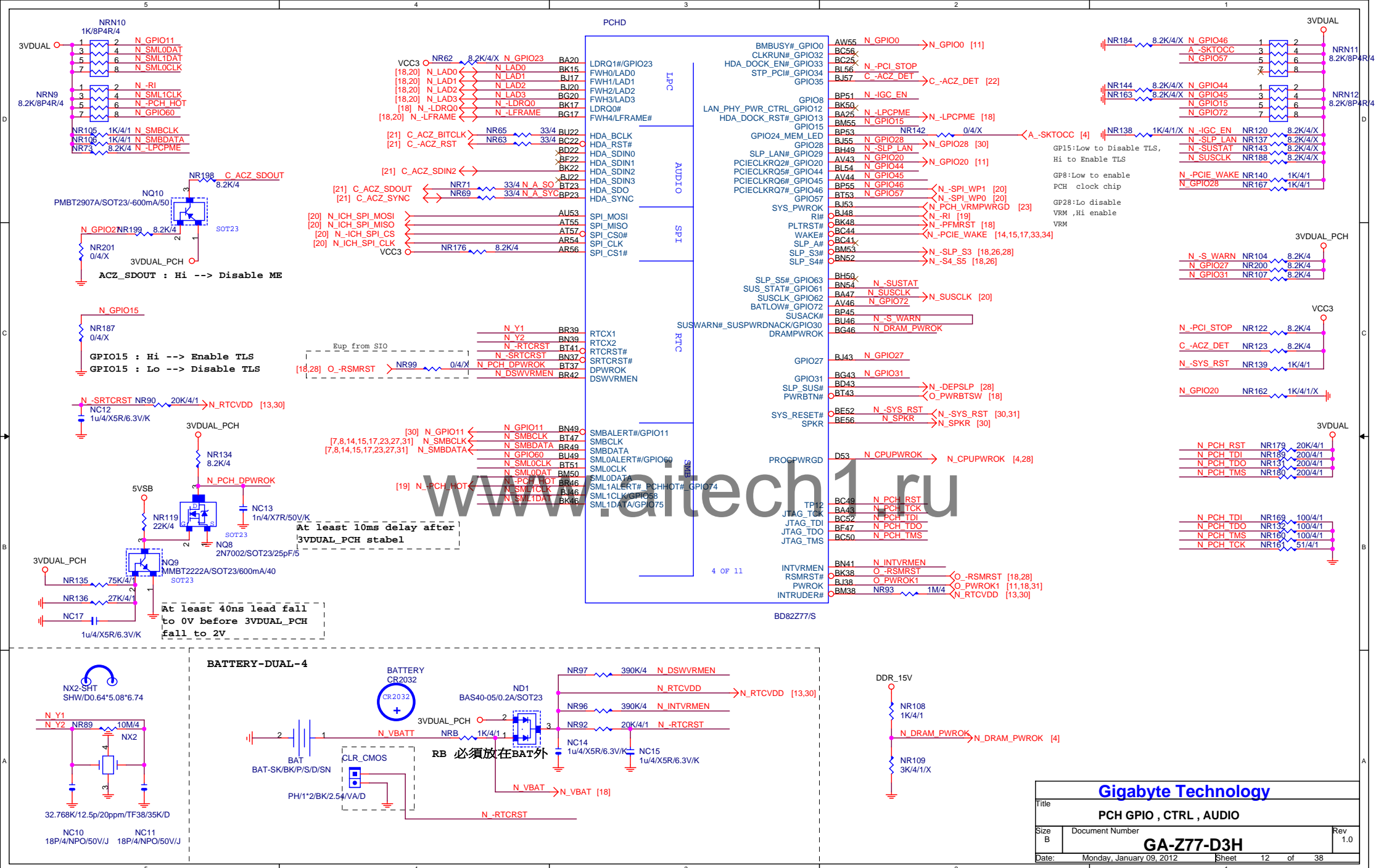
Check if NC for P67 non graphic chip

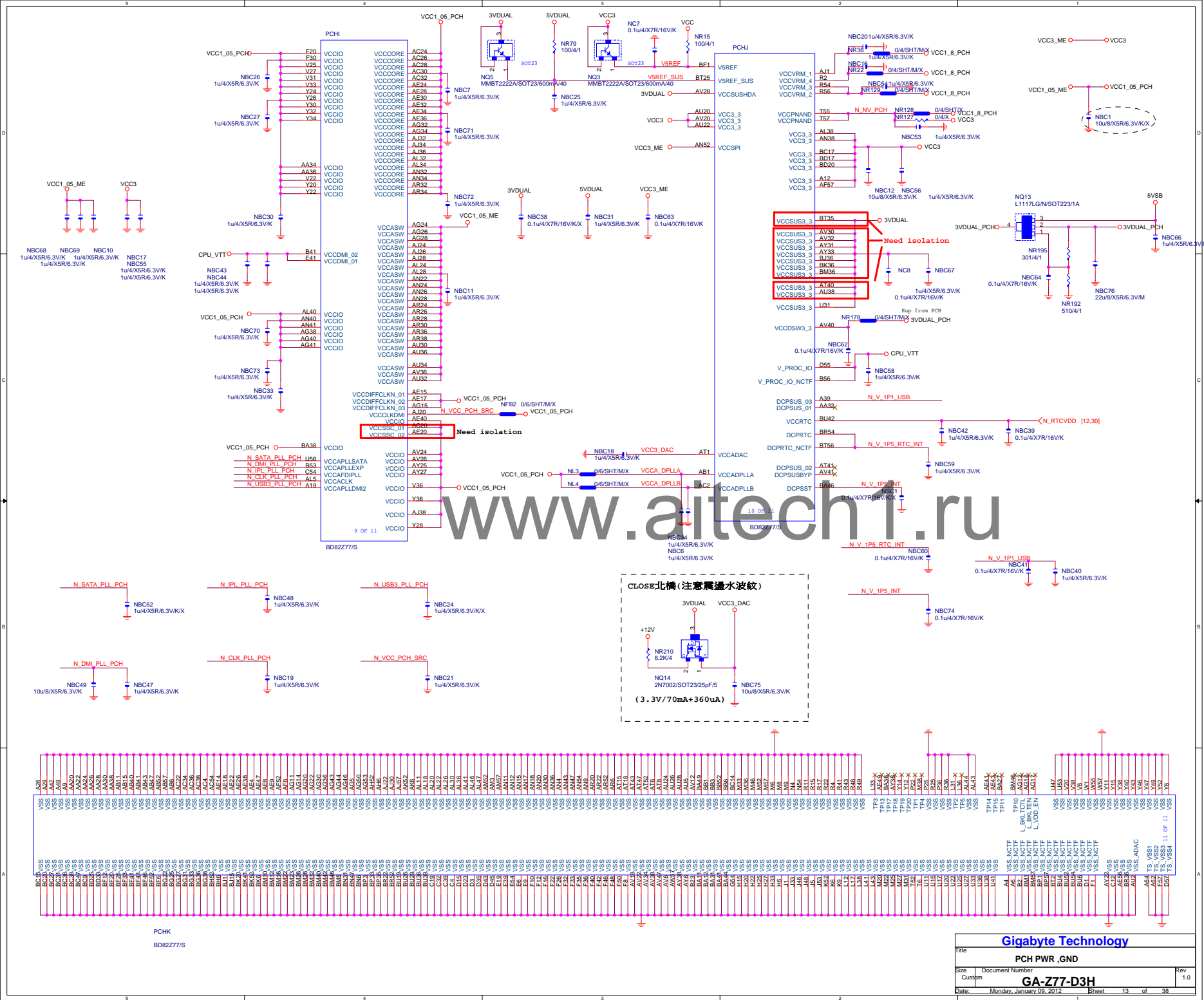


Gigabyte Technology			
Title			
PCH DISPLAY ,CLK BUFFER			
Size	Document Number	Rev	
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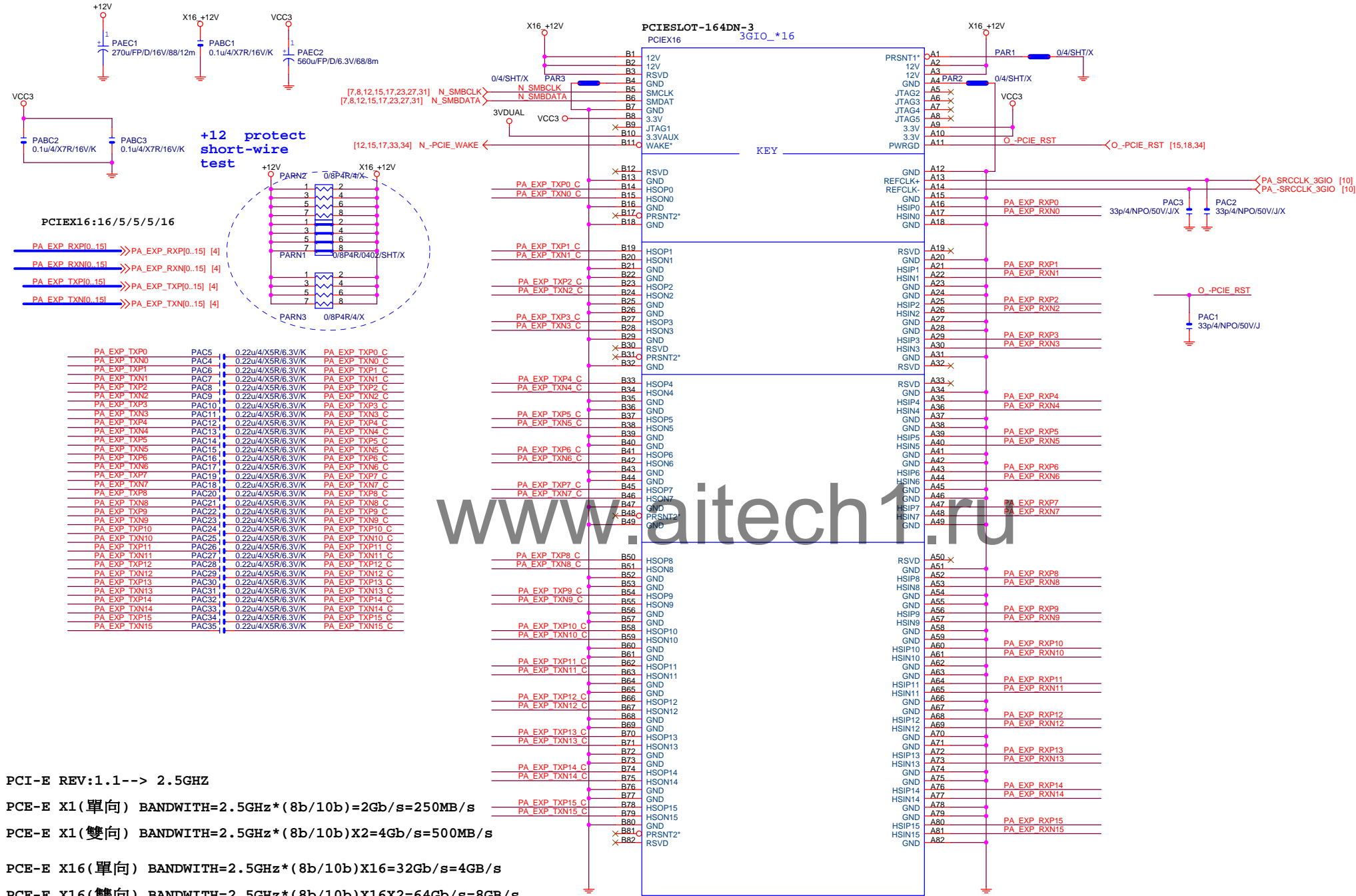
SATA2 : 15/7.5/4.5/7.5/15 (breakout min 8/4/4/4/8)  
Impedance=90 +- 17.5%











PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHz\*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHz\*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz\*(8b/10b)X16=32Gb/s=4GB/s

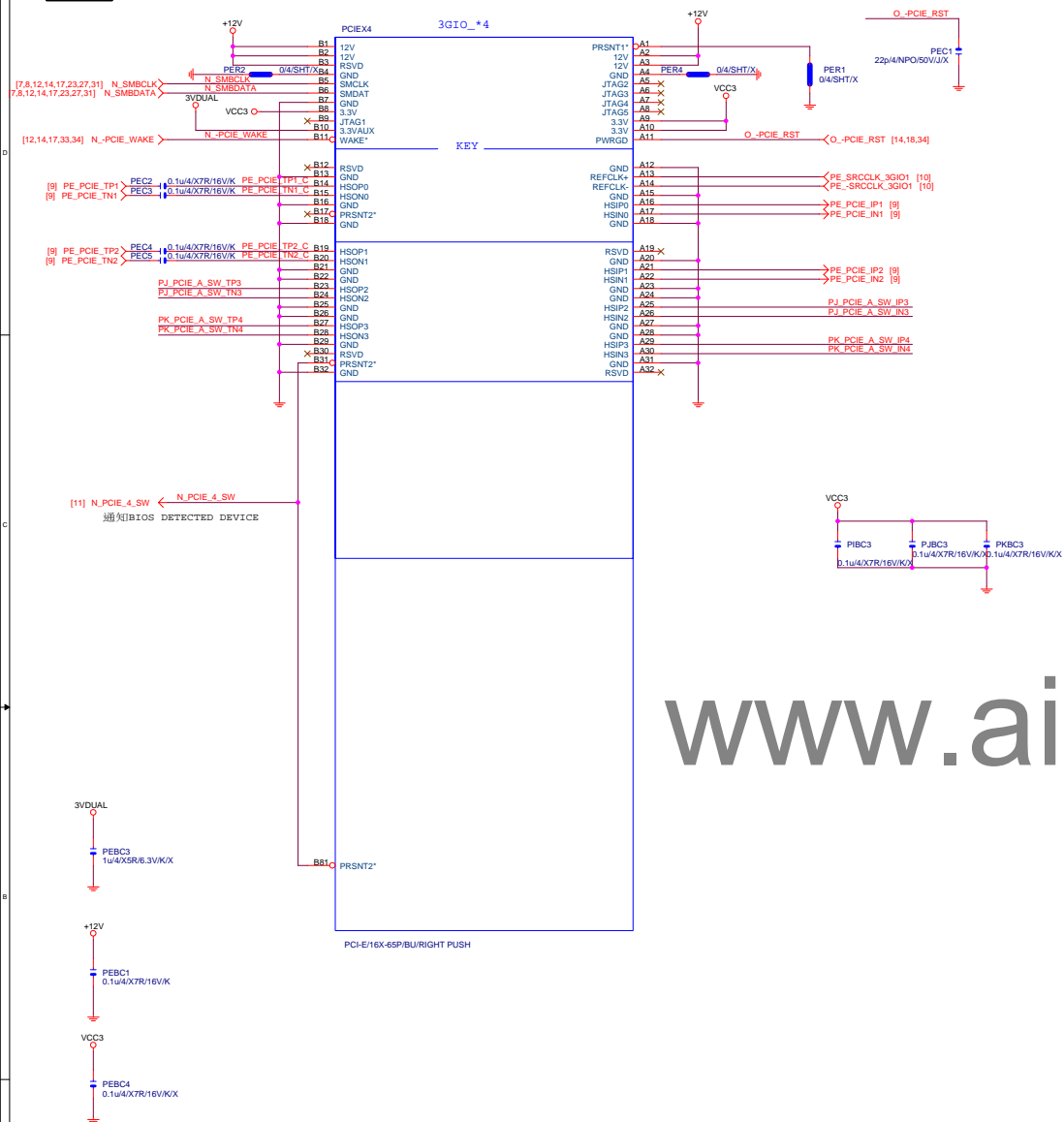
PCE-E X16(雙向) BANDWITH=2.5GHz\*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

Gigabyte Technology			
Title			
PCI EXPRESS * 16			
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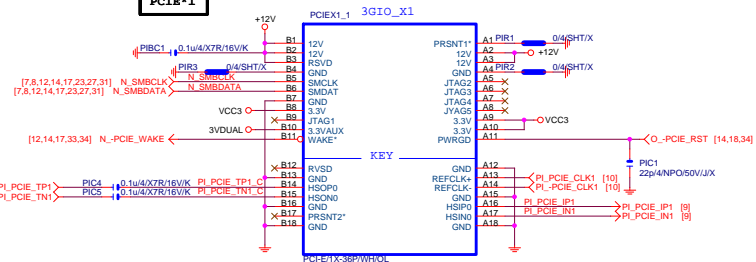


PCIE\*4

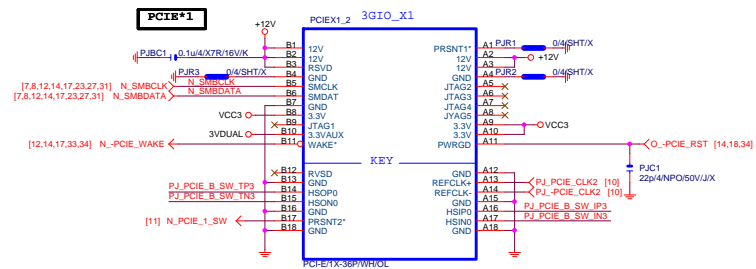


	N_PCIE_4_SW (PCH GPIO38)	PCIE_X1 (SIO_GPIO26)
PCIE_X1, PCIE_X4 --> X1 (Default)	H	H
PCIE_X1_2/PCIE_X1_3 Have devices	H	H
PCIE_X1_2/PCIE_X1_3 No devices	L	L
PCIE_X4 Have devices		
PCIE_X4 -> X4		

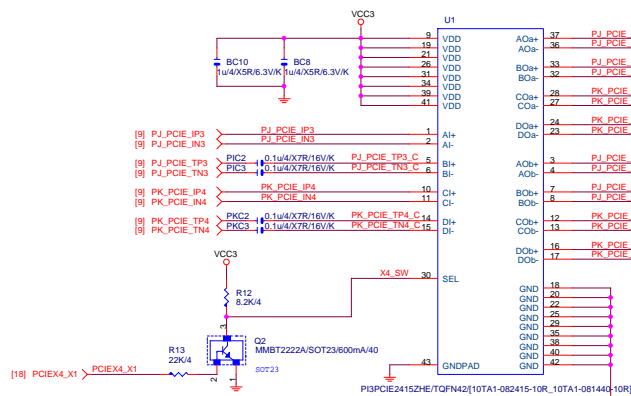
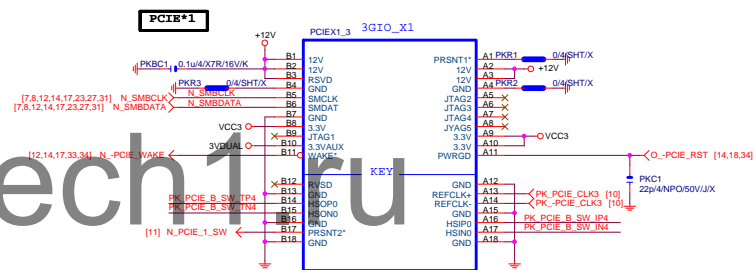
PCIE\*1



PCIE\*1



PCIE\*1



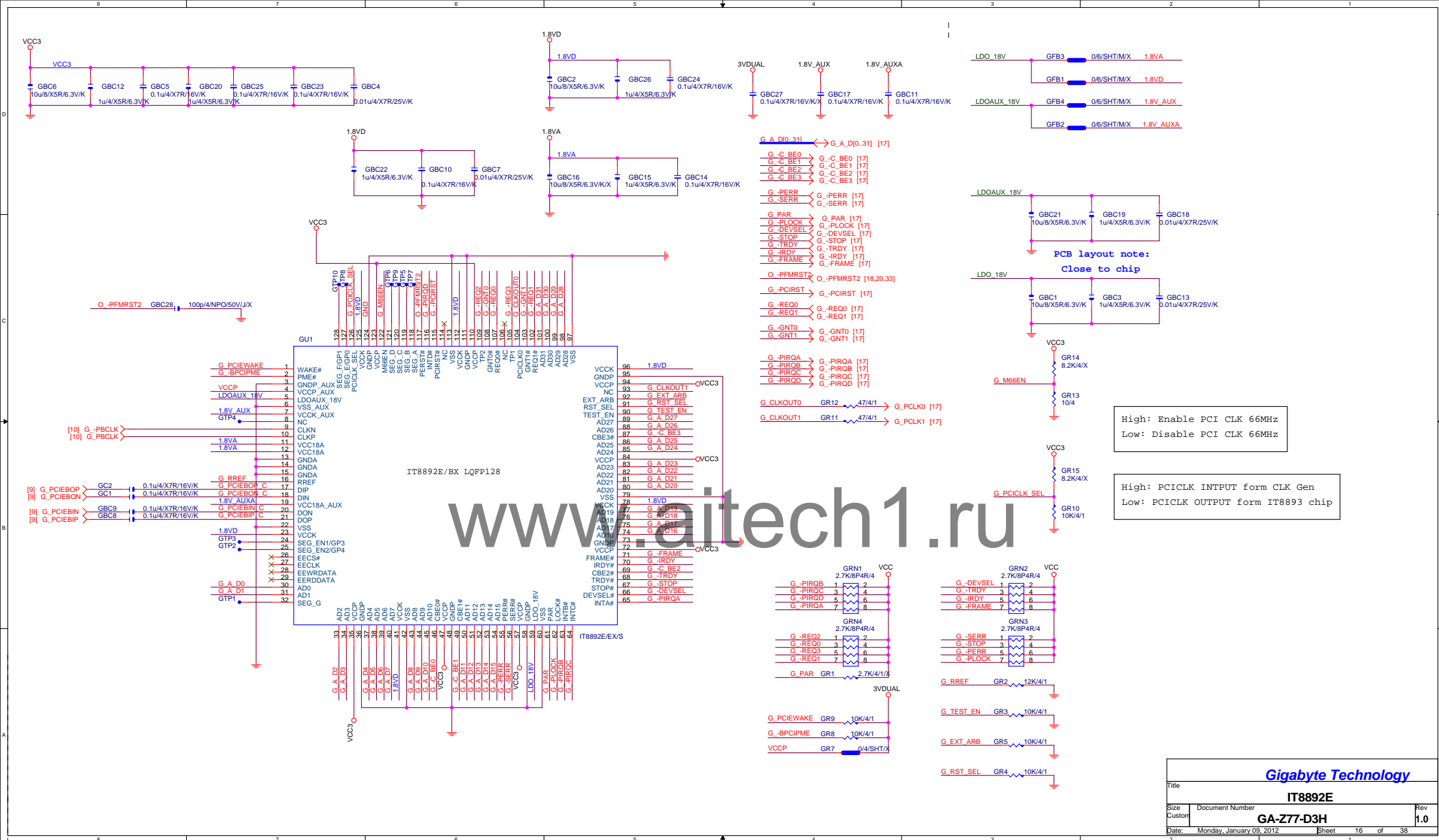
Function	SEL
X1--> x0a	L <sub>1</sub> PCIE_X4 SLOT-->X1
X1--> x0b	H <sub>1</sub> PCIE_X4 SLOT-->X4

Gigabyte Technology

PCIE X1 1.2

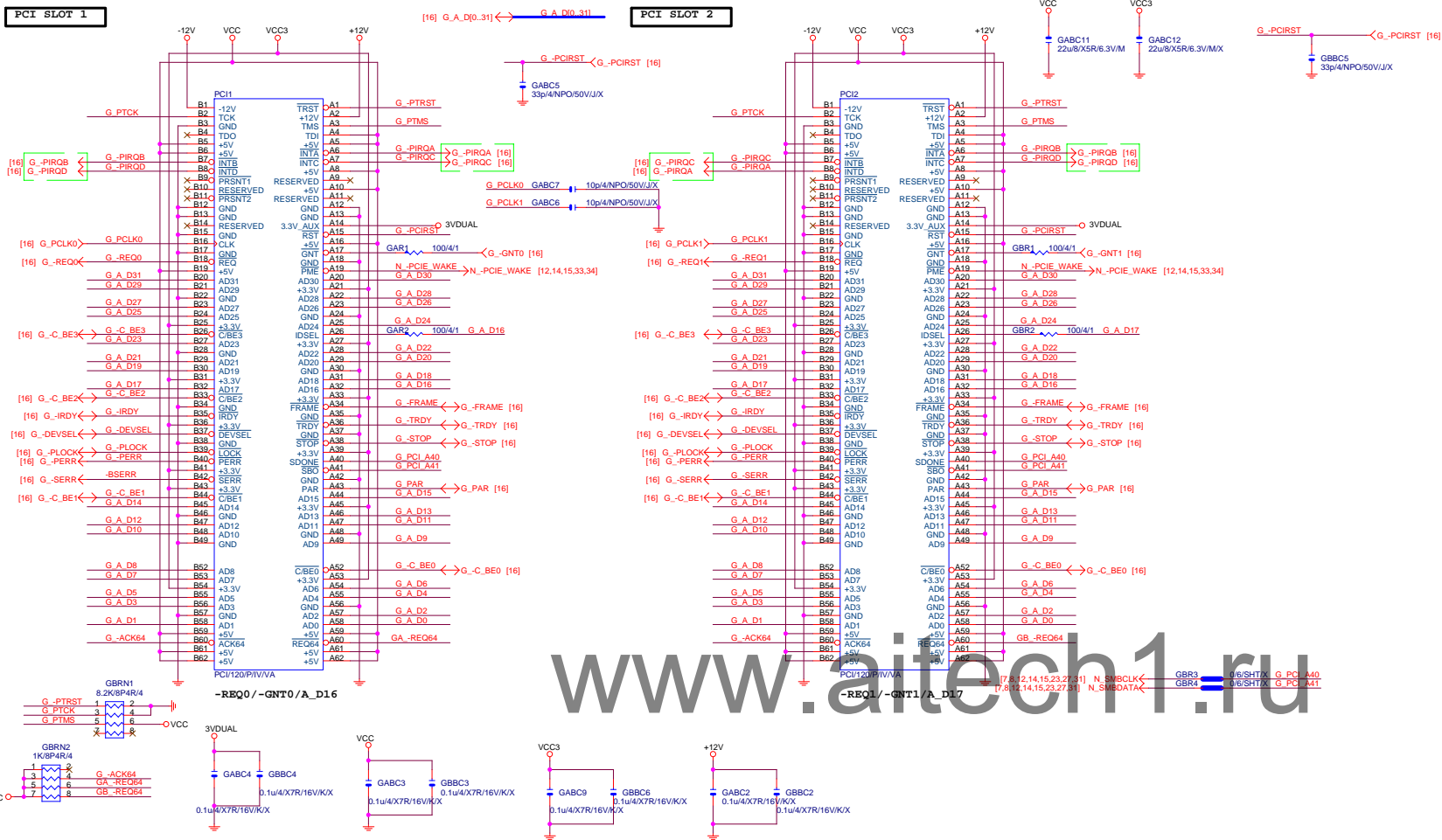
Title	Document Number	Rev
Custom	GA-Z77-D3H	1.0

Date: Monday, January 09, 2012 15 of 38



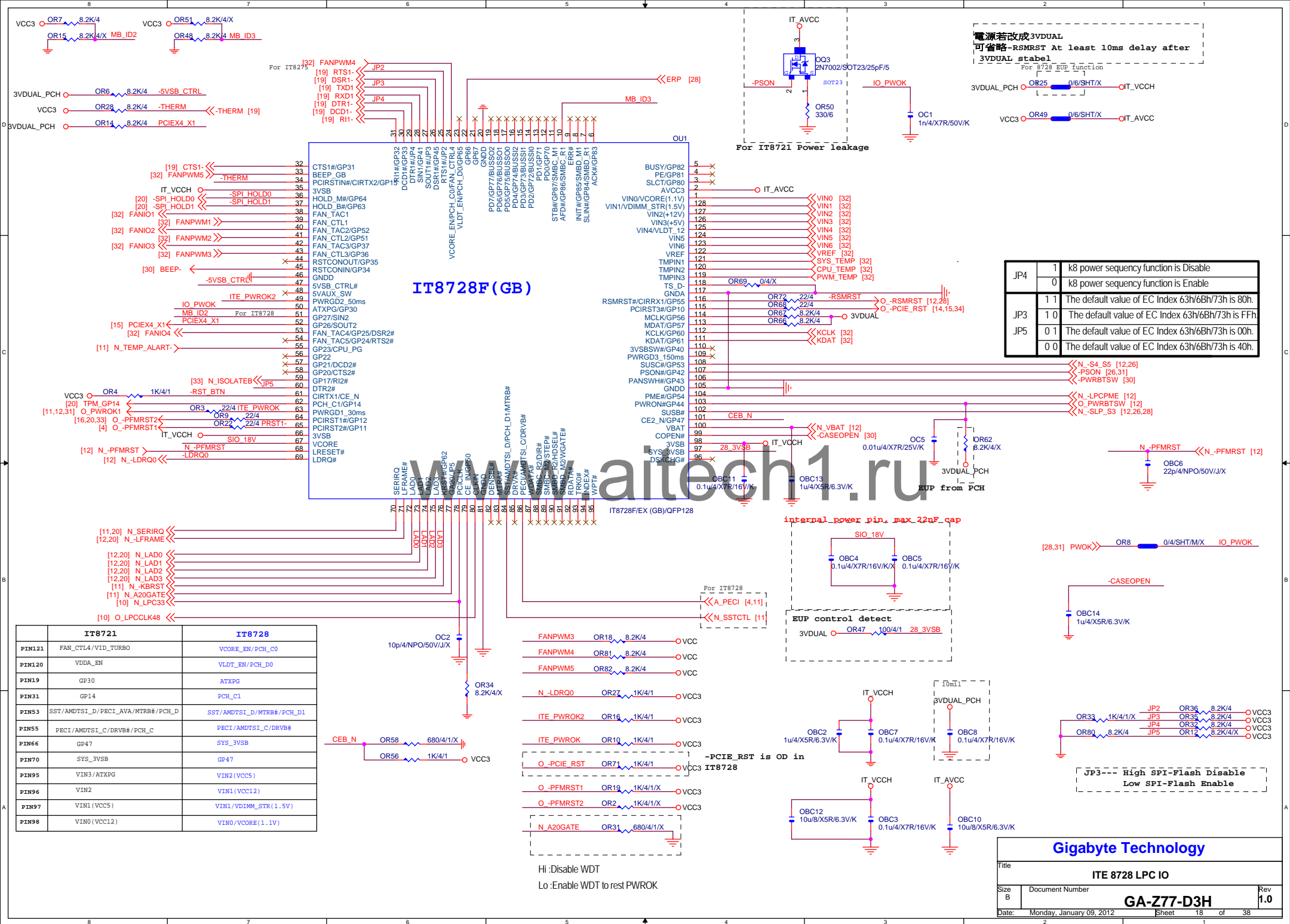
PCI SLOT 1

PCI SLOT 2

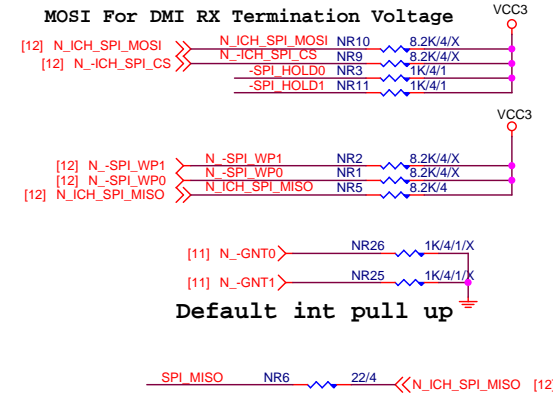
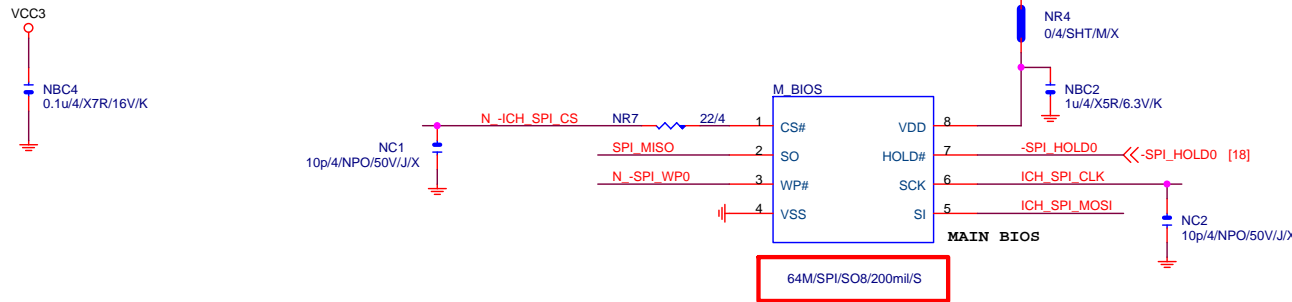


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GIGABYTE™			
PCI SLOT 1&2			
Size	Document Number	Rev	
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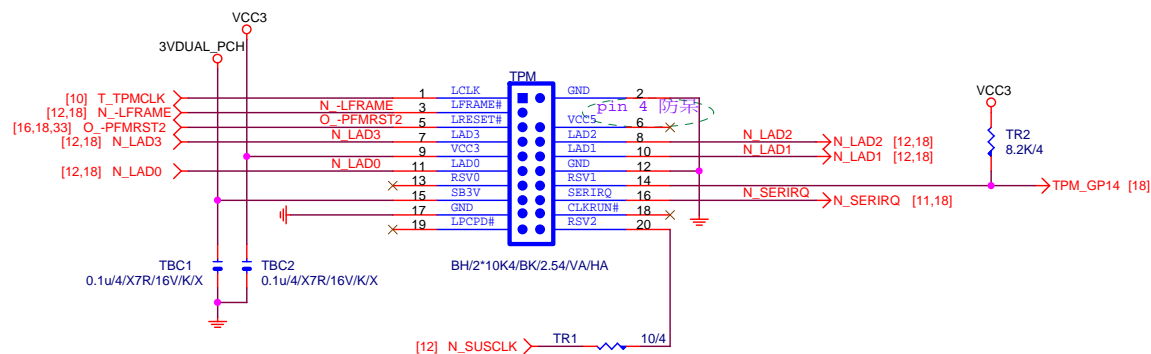




BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating  
 0 means PD 1K

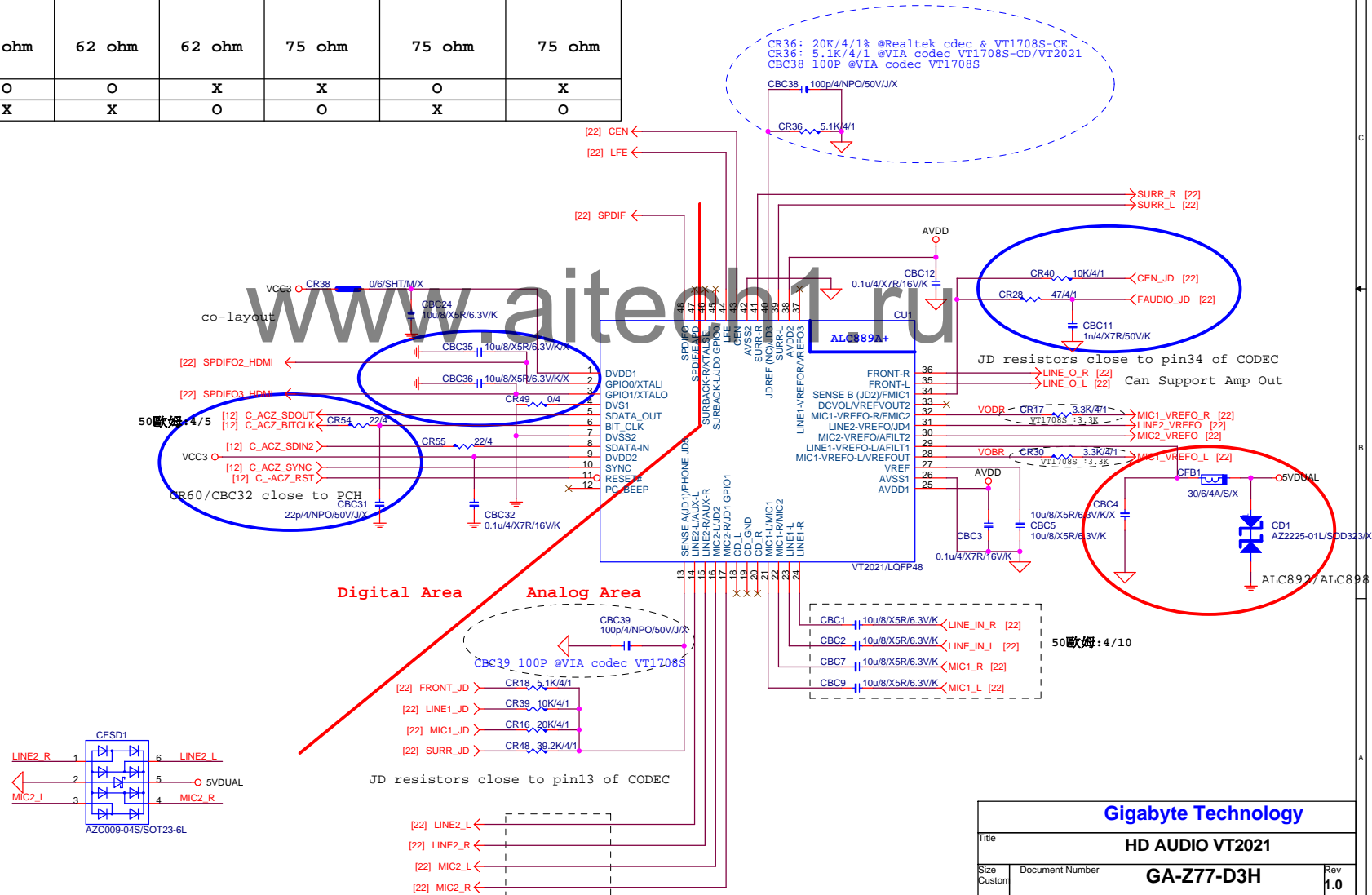
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Gigabyte Technology			
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Size	Document Number	GA-Z77-D3H	
Custom		Rev 1.0	
Date:	Monday, January 09, 2012	Sheet	20 of 38



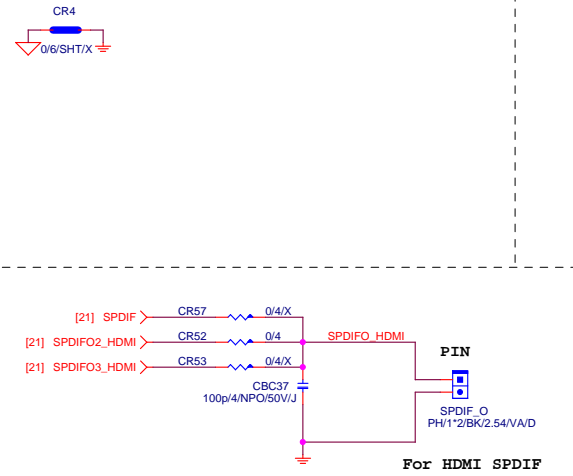
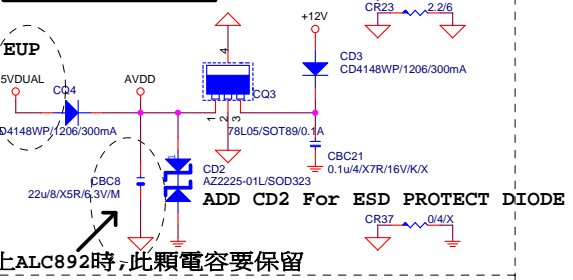
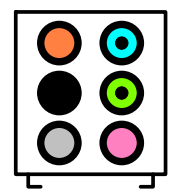
	ALC662	ALC887-VD2	ALC889	VT1708S-CD	VT1708S-CE/ VT1705CF	VT2021
CR49	X	X	O	O	X	O
CBC36	O	O	X	X	O	X
CR28/CBC11	47ohm+1nF	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P	47ohm+1nF
CR52	X	O	O	O	O	O
CR57	O	X	X	X	X	X
CBC1/CBC2	10uF/X5R	10uF/X5R	22uF/X5R	10uF/X5R	10uF/X5R	10uF/X5R
CR36	20K/4/1	20K/4/1	20K/4/1	5.1K/4/1	20K/4/1	5.1K/4/1
CR17/CR30/ CR25/CR15/CR12/CR3/	8.2K/4	8.2K/4	8.2K/4	3.3K/4/1	3.3K/4/1	3.3K/4/1
CBC38/CBC39	X	X	X	100P/4	100P/4	X
CR10/CR8/CR20/CR45/ CR42/CR51/CR27/CR26	22K/4	22K/4	22K/4	10K/4/1	10K/4/1	10K/4/1
CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR2/CR11/ CR14/CR24	62 ohm	62 ohm	62 ohm	75 ohm	75 ohm	75 ohm
CFB1/CD1/CBC4/CBC8	O	O	X	X	O	X
CD2/CD3/CQ3/CQ4	X	X	O	O	X	O



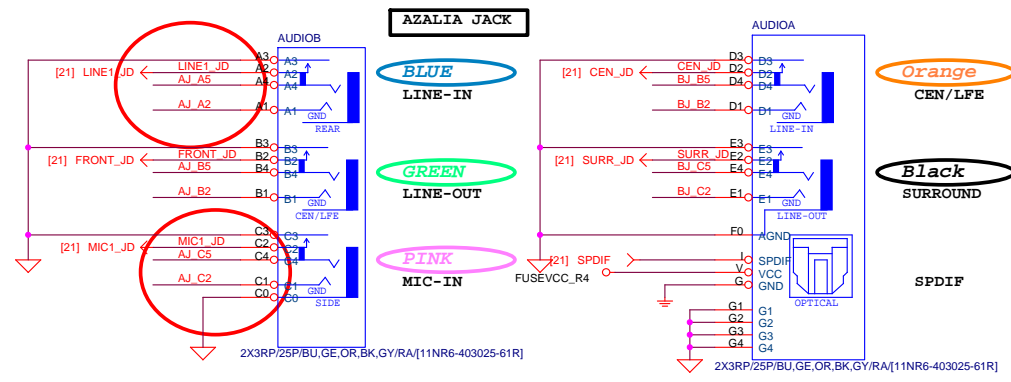
Gigabyte Technology

Title			HD AUDIO VT2021
Size	Document Number	GA-Z77-D3H	
Custom		Rev	1.0
Date:	Monday, January 09, 2012	Sheet	21 of 38

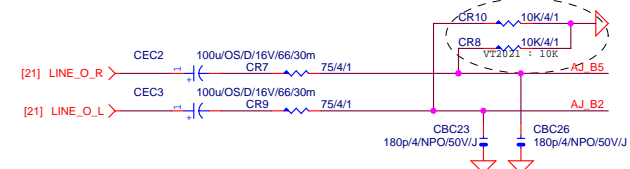
## CODEC POWER/EMI PAD

AZALIA JACK  
BTX AZALIA CONNECTOR

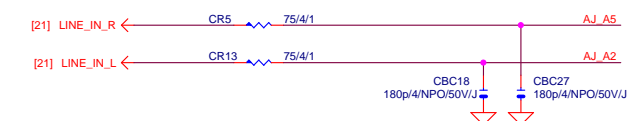
11NR6-403007-21R



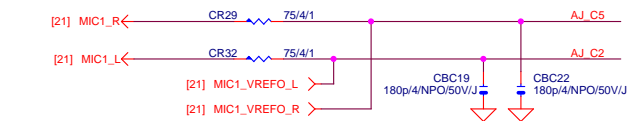
## LINE-OUT



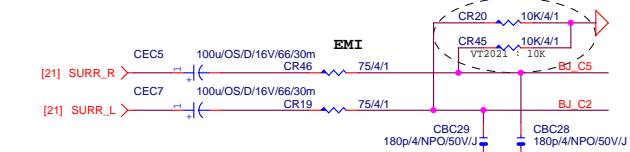
## LINE-IN



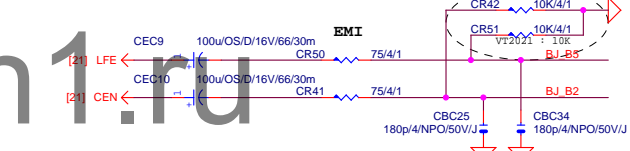
## MIC-IN



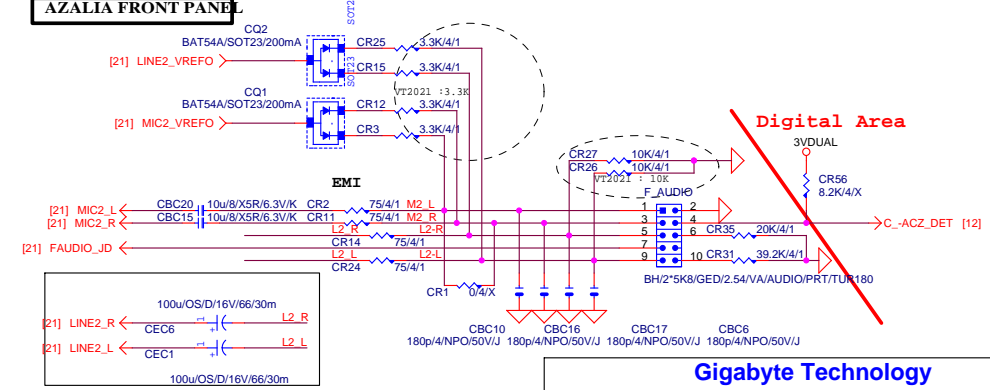
## SURROUND



## CEN/LFE



## AZALIA FRONT PANEL



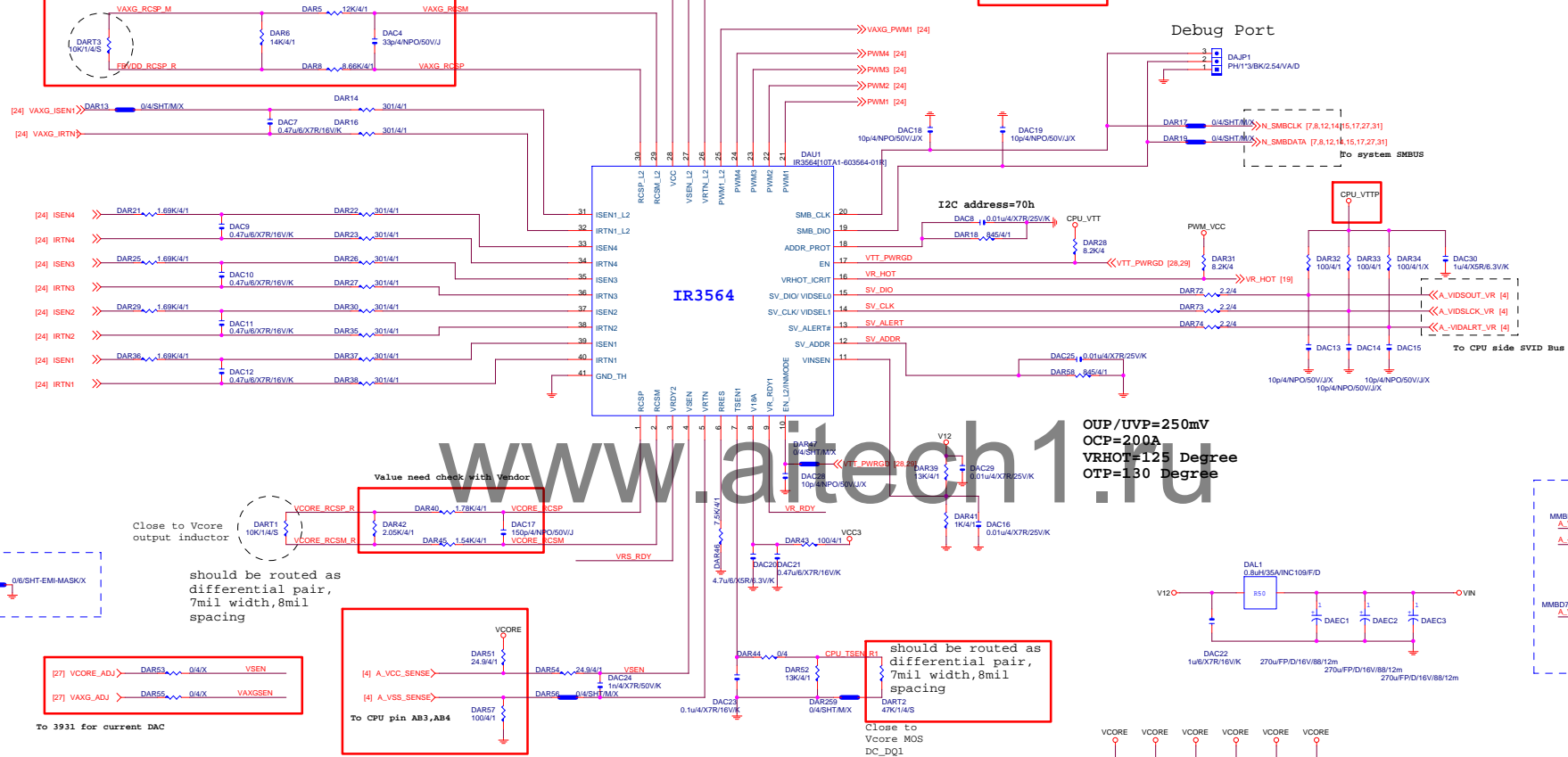
Gigabyte Technology			
Title			
AUDIO JACK			
Size			
Document Number			
GA-Z77-D3H			
Date:			
Monday, January 09, 2012			
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Rev			
1.0			

need 0.1amp , check trace width

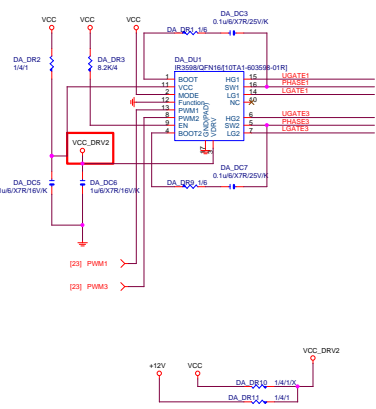
Value need check with Vendor

Close to VSA  
output inductor

should be routed as  
differential pair,  
7mil width,8mil  
spacing

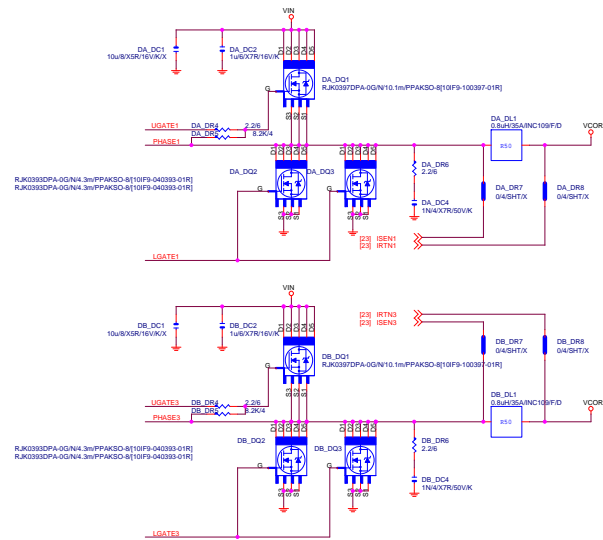


## VCORE Phase 1,3

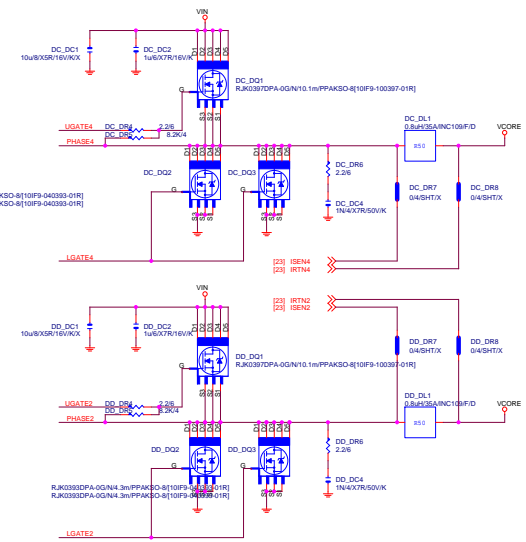
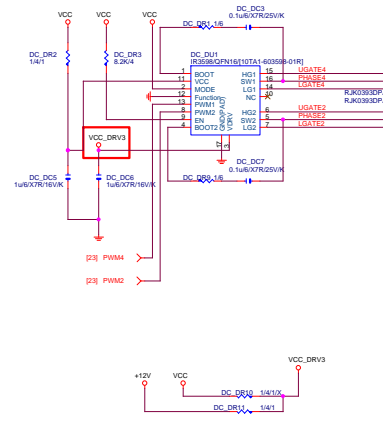


Pin	Mode	Pin	Mode	Pin	Mode
1	BOOT	16	SW1	16	SW1
2	VCC	17	SW2	17	SW2
3	MODE	18	SW3	18	SW3
4	PGM1	19	SW4	19	SW4
5	PGM2	20	SW5	20	SW5
6	PGM3	21	SW6	21	SW6
7	PGM4	22	SW7	22	SW7
8	PGM5	23	SW8	23	SW8
9	PGM6	24	SW9	24	SW9
10	PGM7	25	SW10	25	SW10
11	PGM8	26	SW11	26	SW11
12	PGM9	27	SW12	27	SW12
13	PGM10	28	SW13	28	SW13
14	PGM11	29	SW14	29	SW14
15	PGM12	30	SW15	30	SW15

In Quad mode, I2C pin10 link to I2C pin11  
I2C pin10 link to I2C pin11 without pin

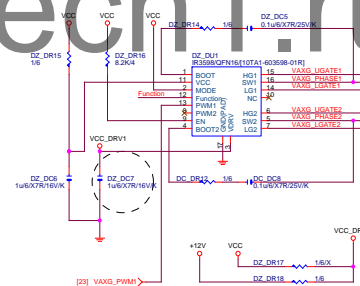


## VCORE Phase 4,2

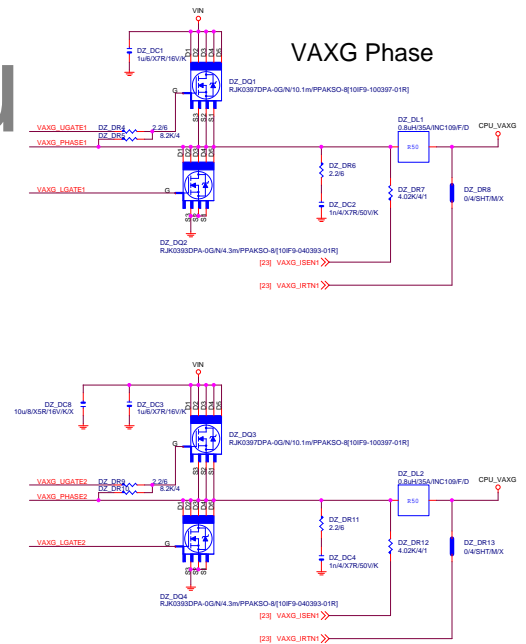


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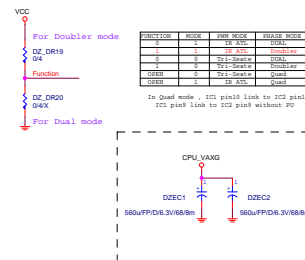
## VAXG PHASE 1,2



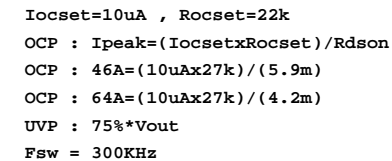
## VAXG Phase



## MOS HEATSINK



## CPU\_VTT

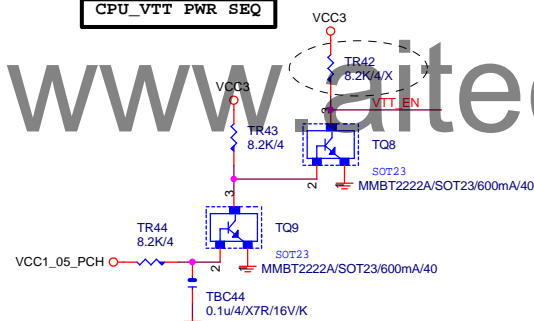


CPU_VTT	PWR	SEQ
0	0	0
0	0	1
0	0	2
0	0	3
0	0	4
0	0	5
0	0	6
0	0	7
0	0	8
0	0	9
0	0	10
0	0	11
0	0	12
0	0	13
0	0	14
0	0	15
0	0	16
0	0	17
0	0	18
0	0	19
0	0	20
0	0	21
0	0	22
0	0	23
0	0	24
0	0	25
0	0	26
0	0	27
0	0	28
0	0	29
0	0	30
0	0	31
0	0	32
0	0	33
0	0	34
0	0	35
0	0	36
0	0	37
0	0	38
0	0	39
0	0	40
0	0	41
0	0	42
0	0	43
0	0	44
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0	0	46
0	0	47
0	0	48
0	0	49
0	0	50
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0	0	118
0	0	119
0	0	120
0	0	121
0	0	122
0	0	123
0	0	124
0	0	125
0	0	126
0	0	127
0	0	128
0	0	129
0	0	130
0	0	131
0	0	132
0	0	133
0	0	134
0	0	135
0	0	136
0	0	137
0	0	1

	VTT_SEL
HI	1.05V
LO	1.0V

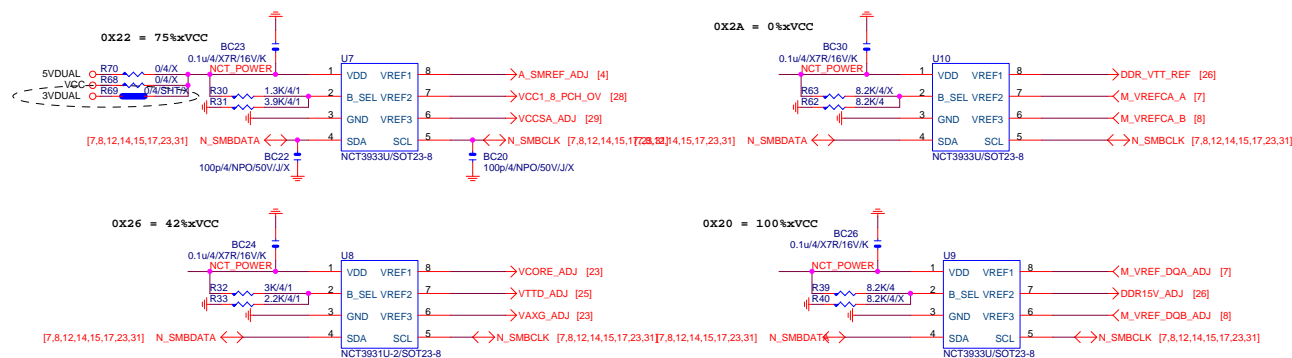
$$0.8 \cdot (1 + R_S/R_O) = V_{out}$$

$$0.8 \cdot [1 + 1.1K/3K] =$$

$$1.09V$$








NCT3933	0X2A	0X20	0X22	0X26
VREF1	DDRVTT	VREF_DDRA_DQ	SMREF	VCORE
VREF2	VREF_DDRA_CA	DDR15V	VCC1_8_PCH	CPU_VTT
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	VCCSA	VAXG

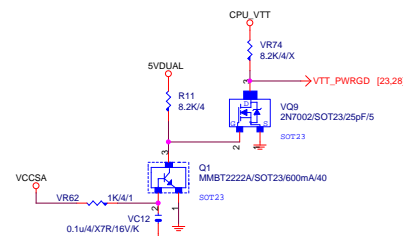
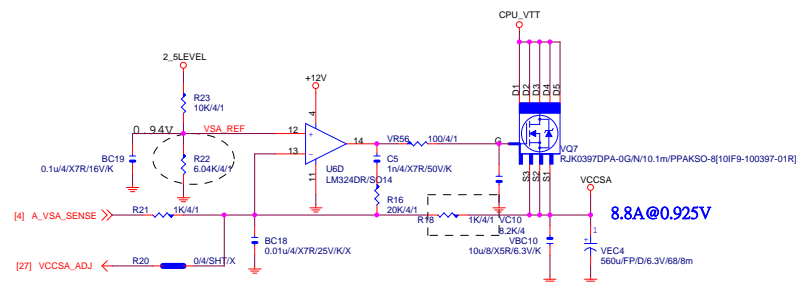
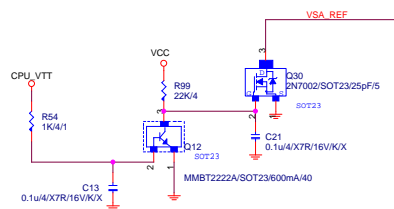
Gigabyte Technology		
Title CPU CORE VR-2		
Size Custom	Document Number GA-Z77-D3H	Rev 1.0
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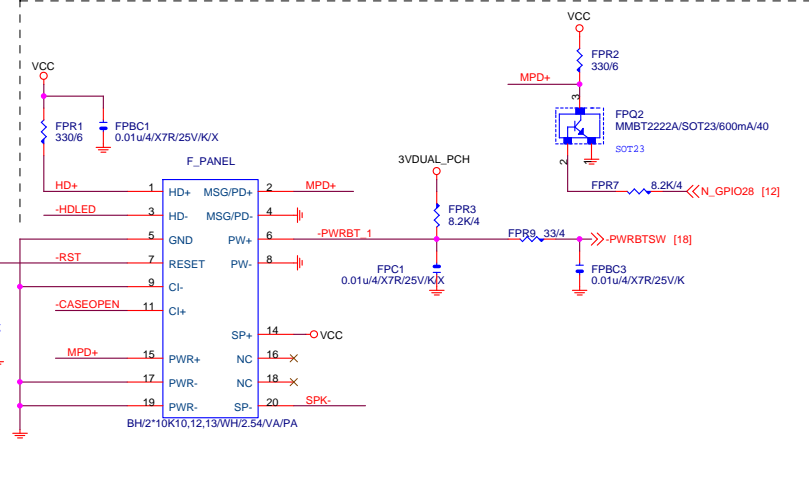
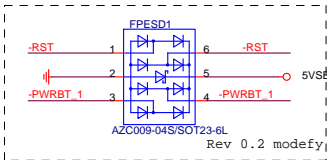
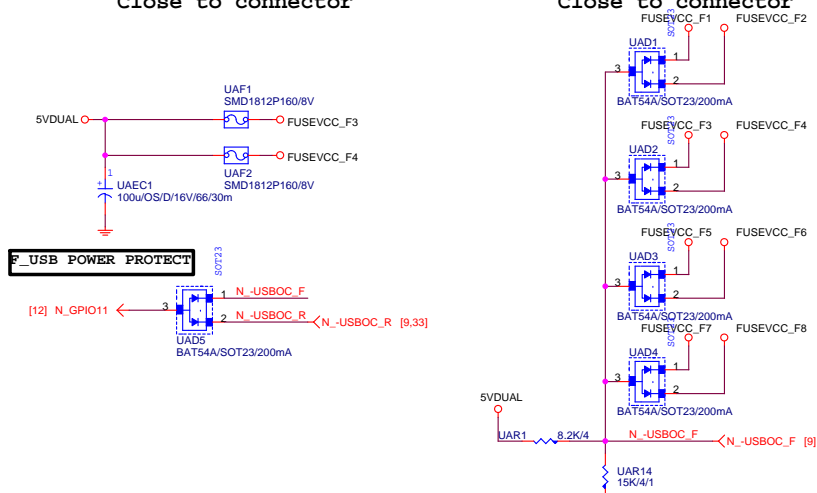
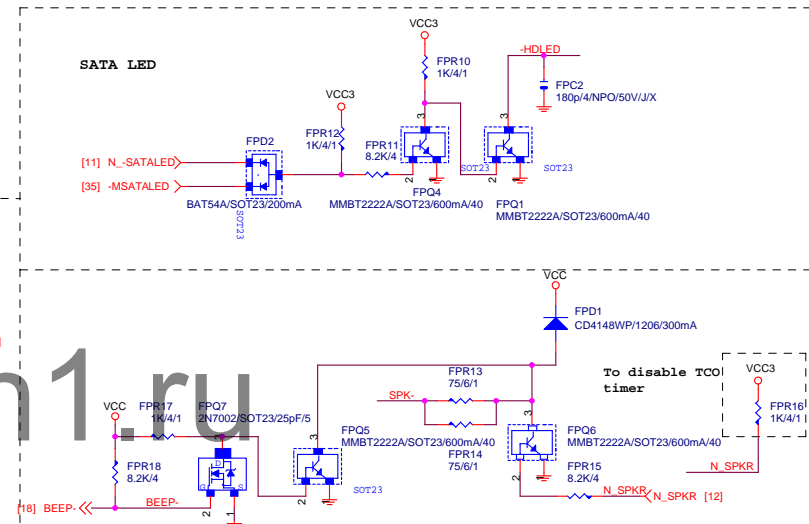
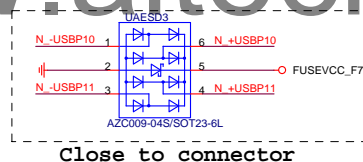
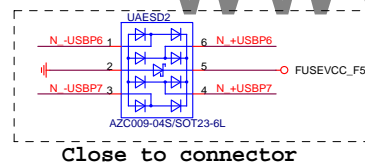
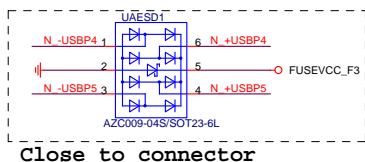
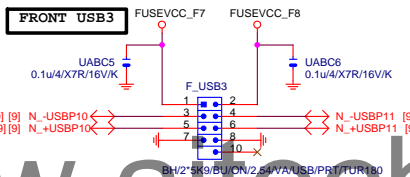
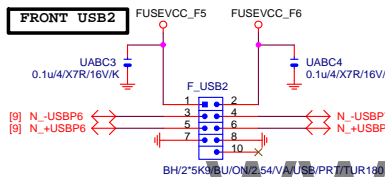
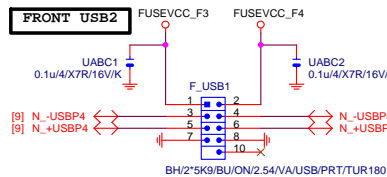
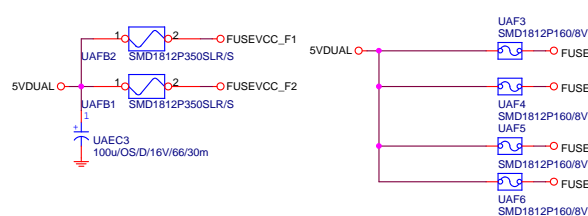
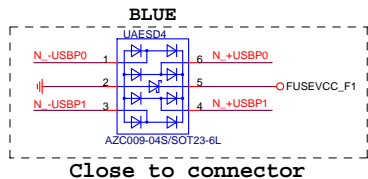
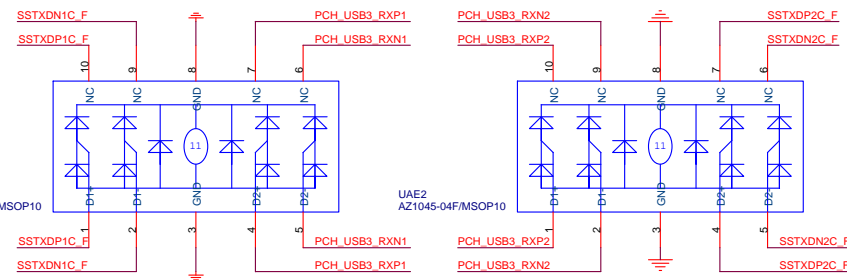
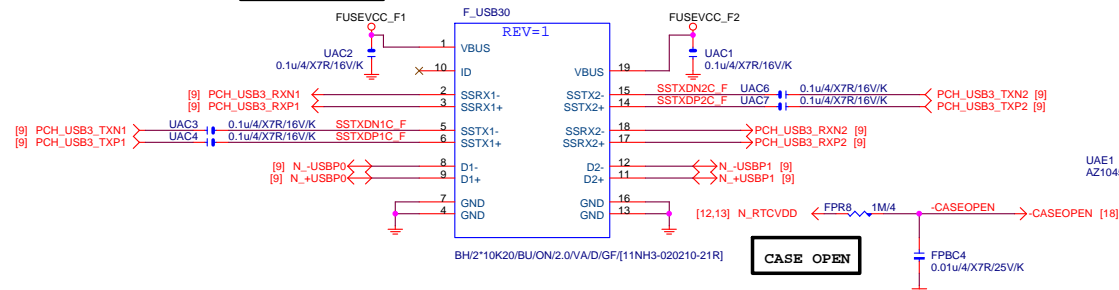
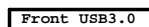


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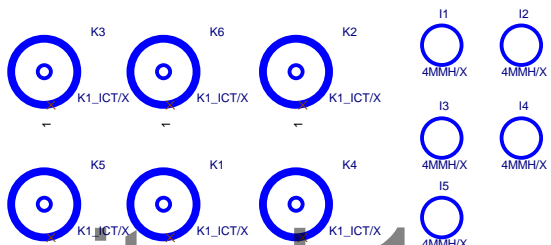
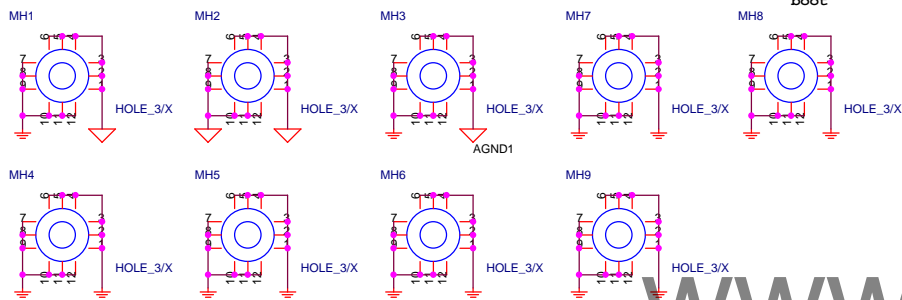
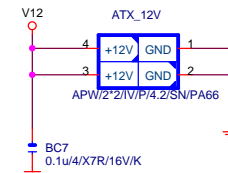
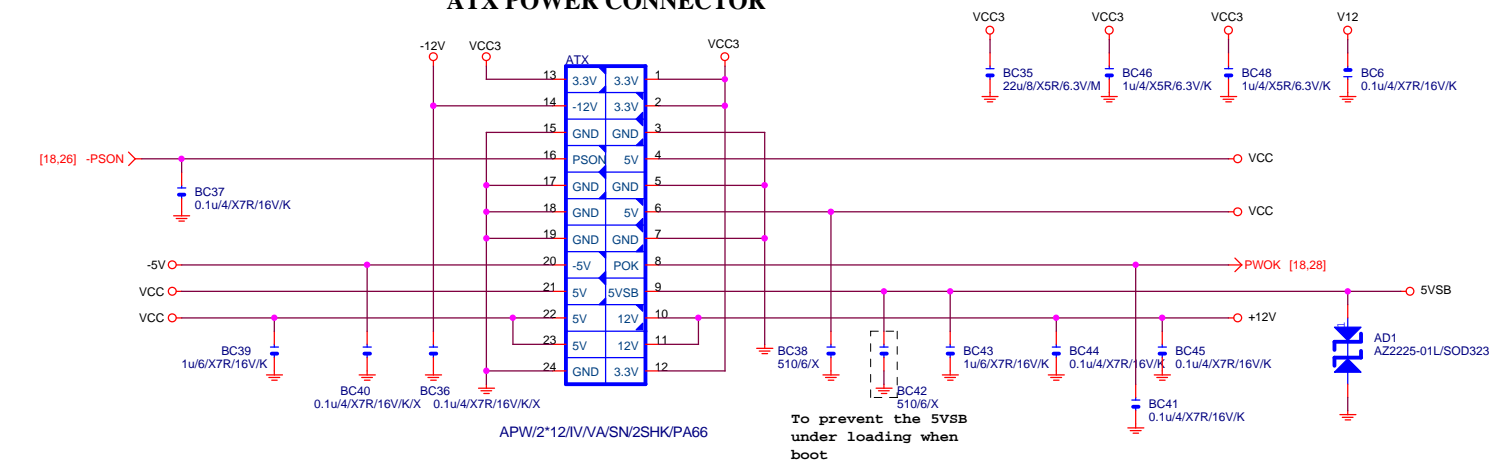
VCC\_SA



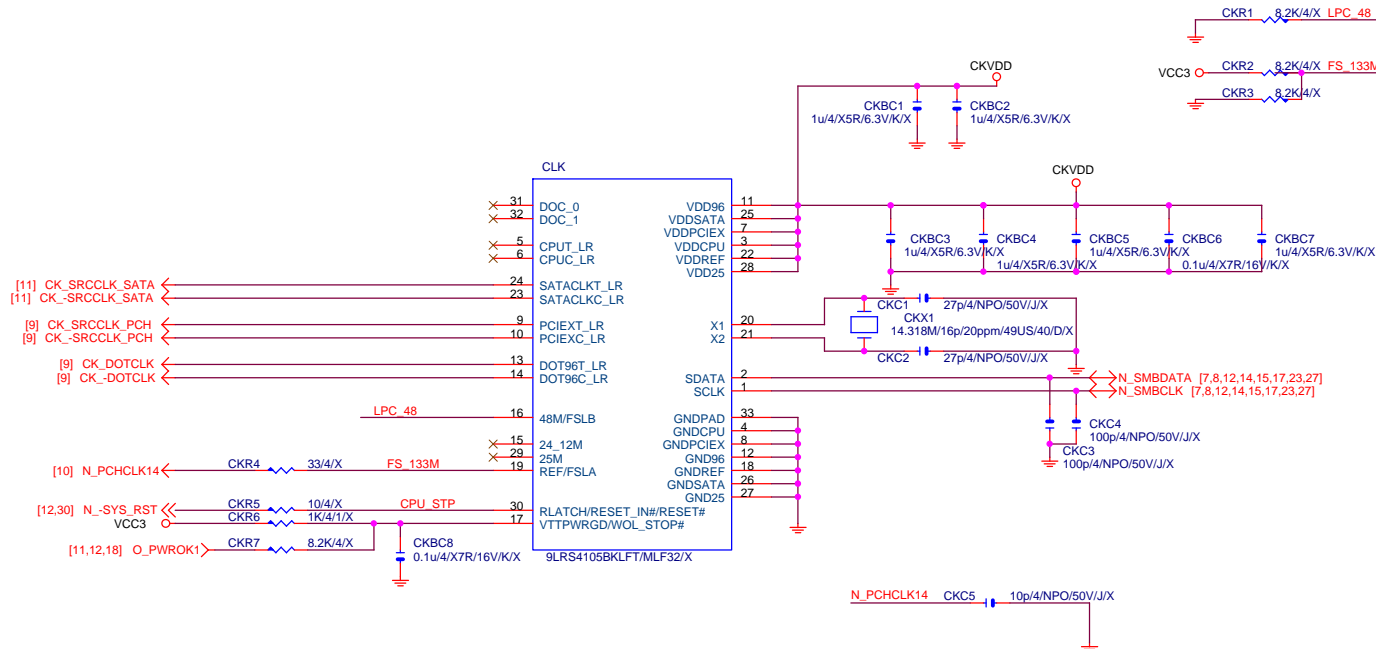
Gigabyte Technology			
CPU VTT PWM_ISL6312			
File	Document Number	Rev	
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# ATX POWER CONNECTOR

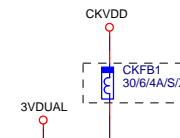


## CLK GEN



## CPU Frequency Selection

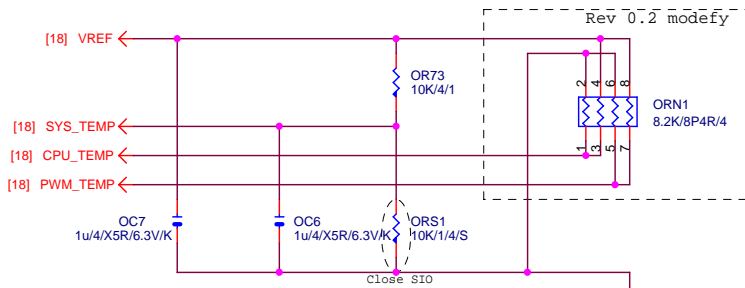
FS	CPU
0	100M <Default>
1	133M



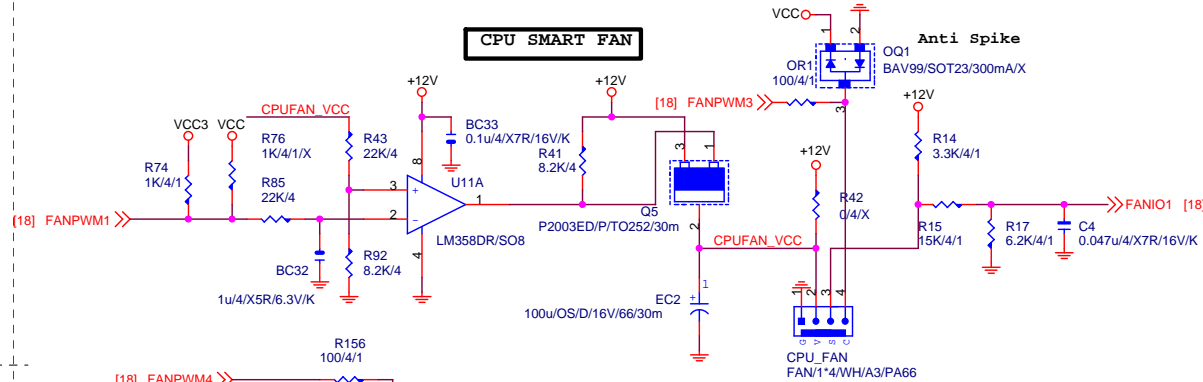
## Gigabyte Technology

Title		
ATX POWER CONNECTOR		
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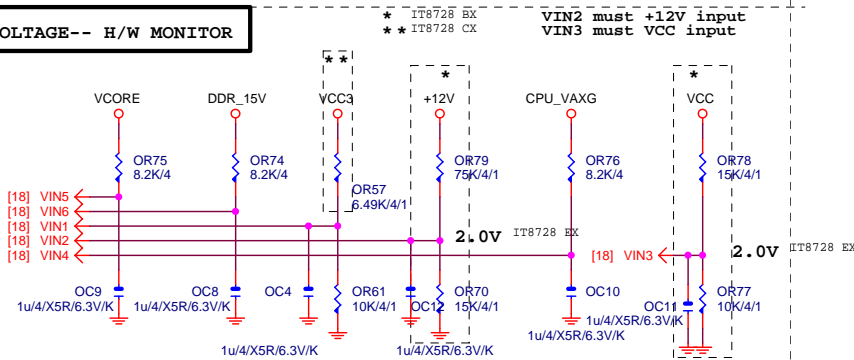
## TEMP H/W MONITOR



## CPU SMART FAN

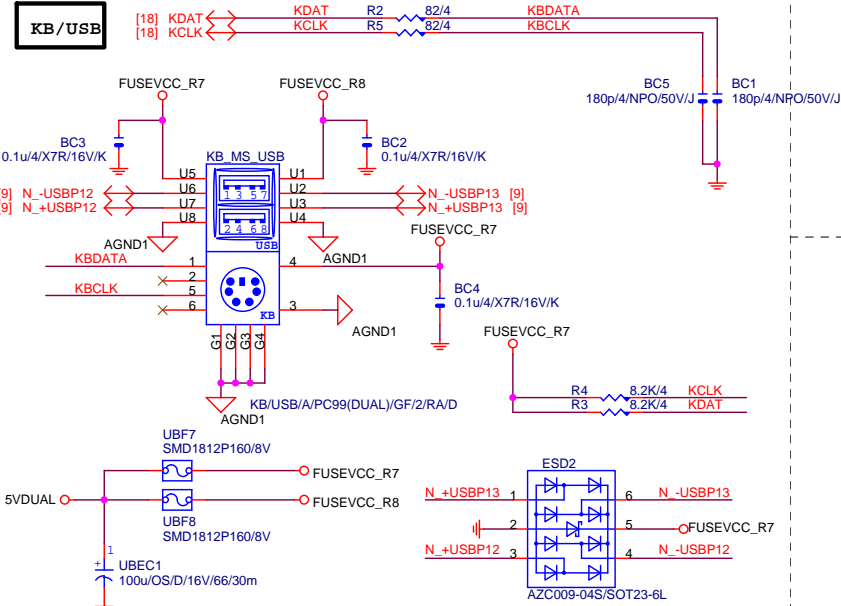


## VOLTAGE-- H/W MONITOR

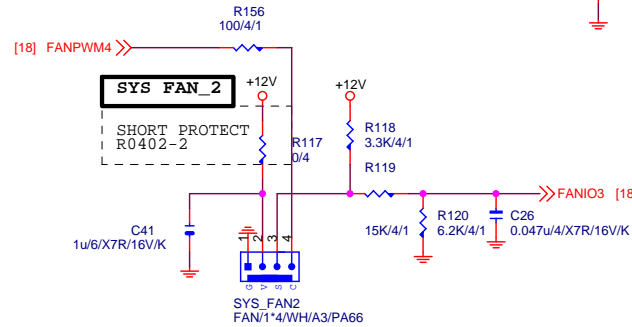


The division voltage of VIN2 & VIN3 must be around 2.9V

## KB/USB

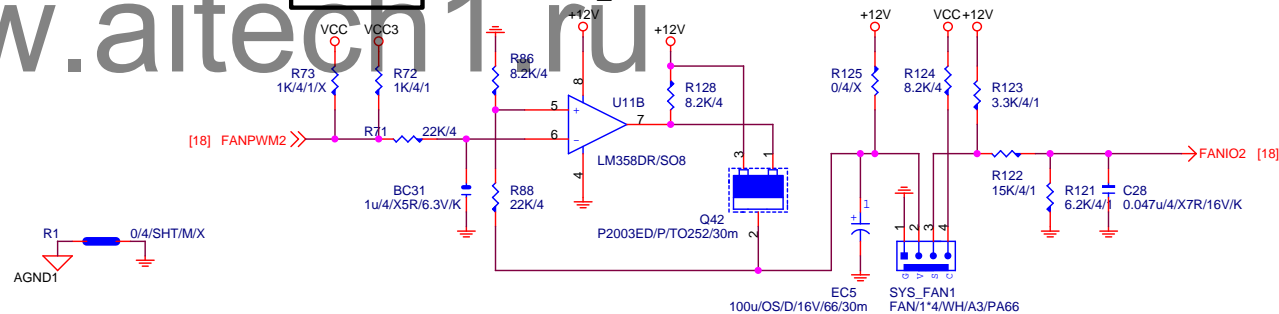


## SYS FAN\_2



## SYS FAN\_1

## Linear SYS\_FAN

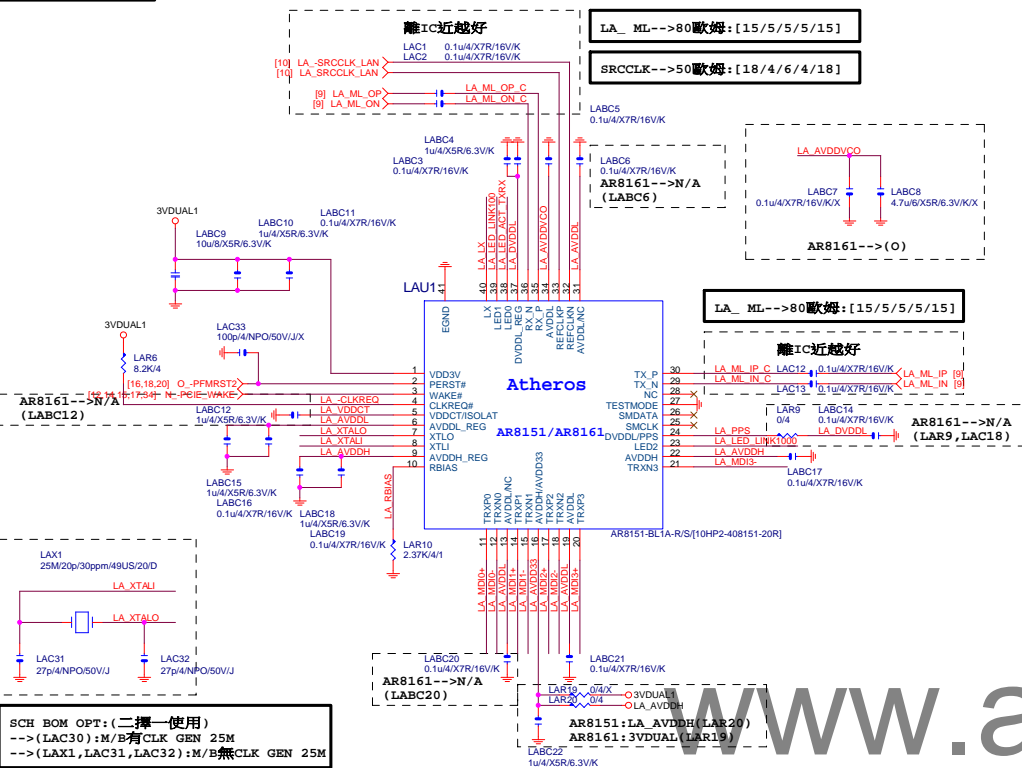


Gigabyte Technology

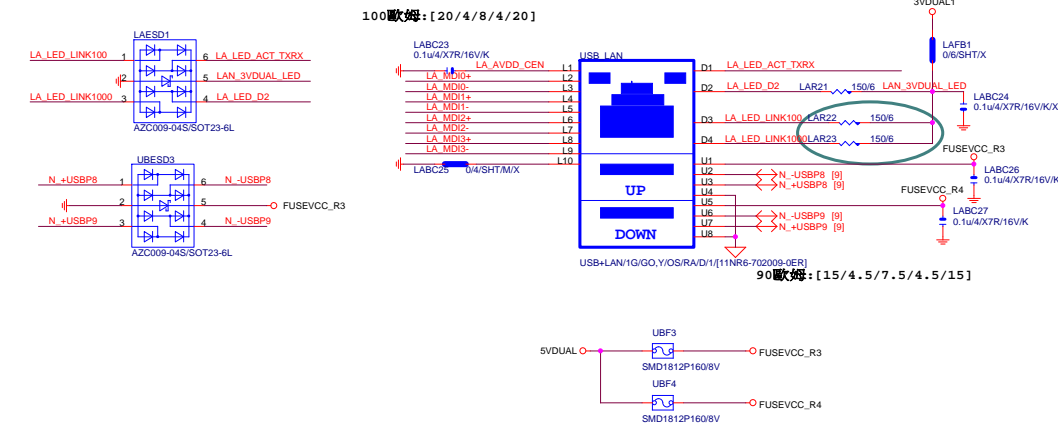
Title			
HWM,KB/MS, FAN CTRL			
Size	Document Number	Rev	
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LAN:AR8151/AR8161

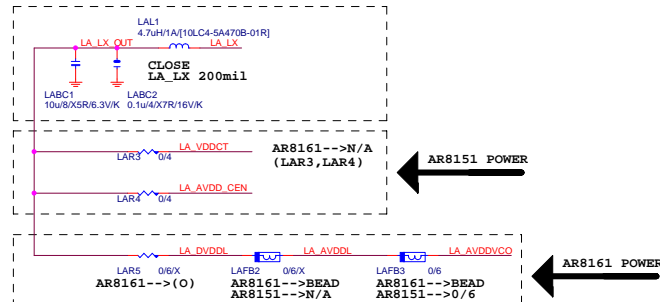


## USB30\_LAN CONNECTOR



## LAN POWER

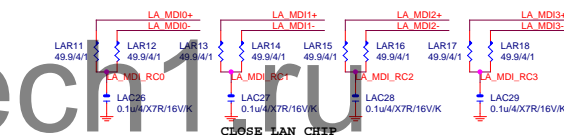
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NEW DESIGN ONLY FOR INTERNAL SWR
AR8151:LAR3(O),LAR5(X)
AR8161:LAR5(O),LAR3/LAR4(X)
```

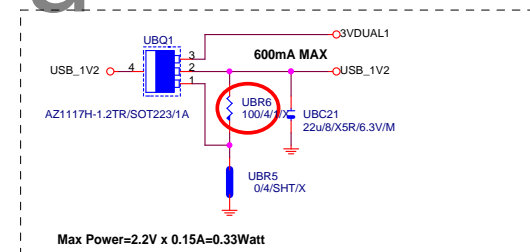
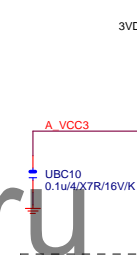
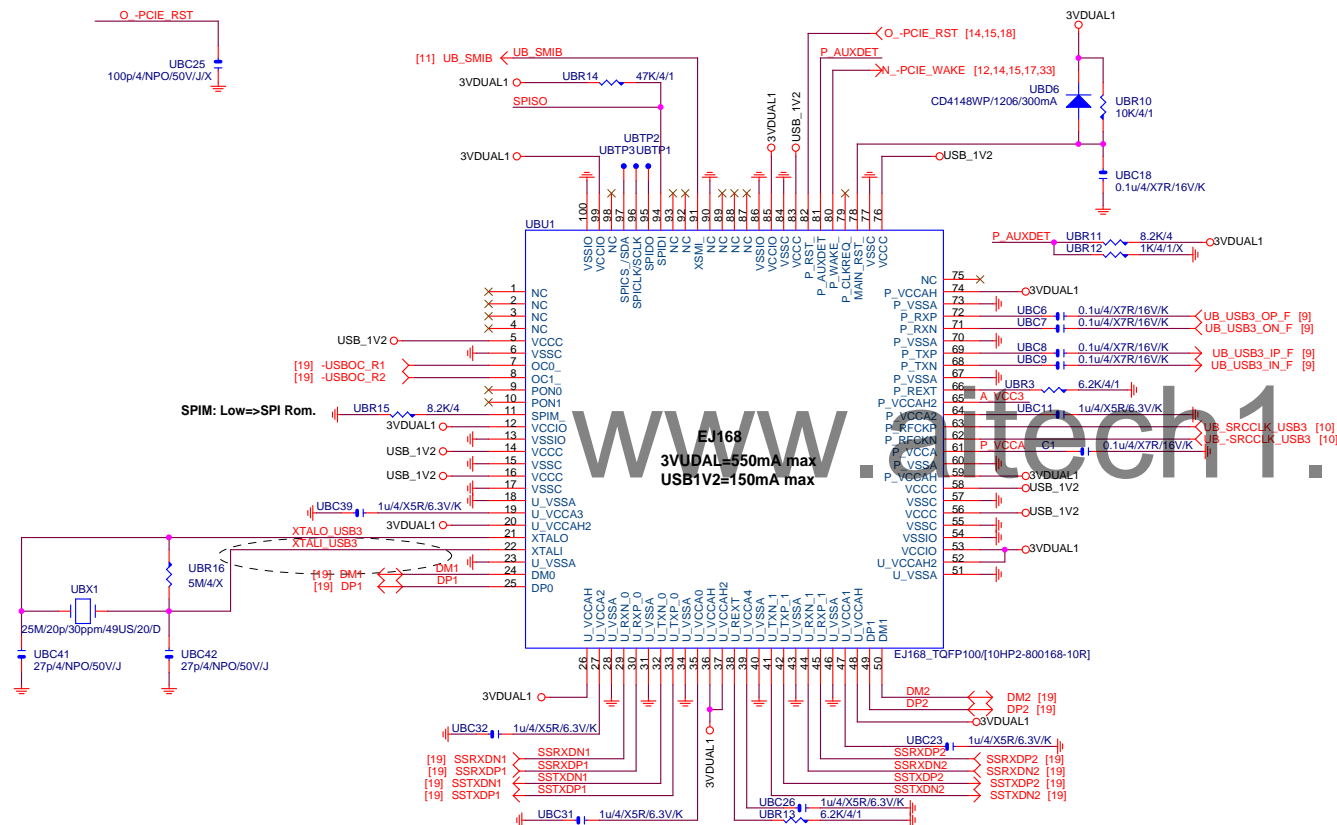
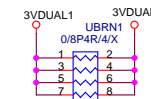
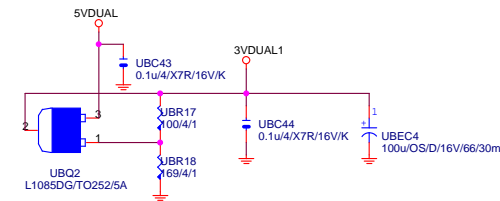
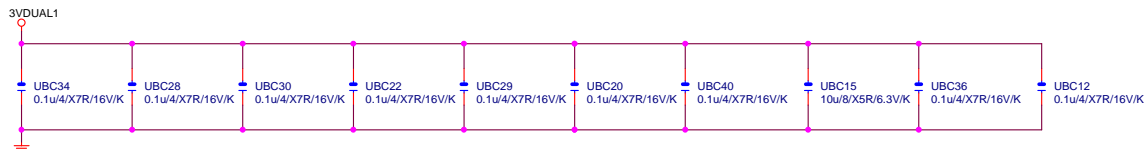


### Power domain chart

	AR8151	AR8161
AVDD33	N/A	3.3V
VDD33	3.3V	3.3V
AVDDH	2.7V	2.7V
AVDDL/DVDDL	1.1V	1.1V
VDDCT	1.7V	

MDI : AR8161--&gt;N/A

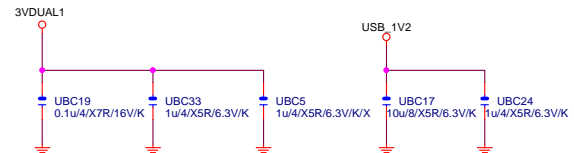
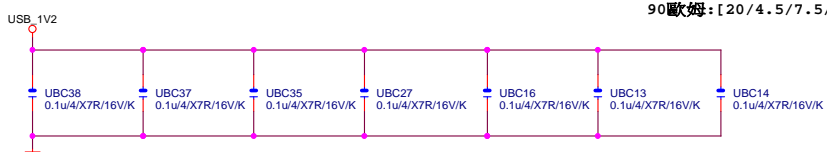




Max Power=2.2V x 0.15A=0.33Watt

AZ1117H-1.2TR/SOT223/1A-->UR17:0/4,UR16:N/A [1.2V]

L1117LG/N/SOT223/1A-->UR17:0/4,UR16:100/4/1 [1.25V]

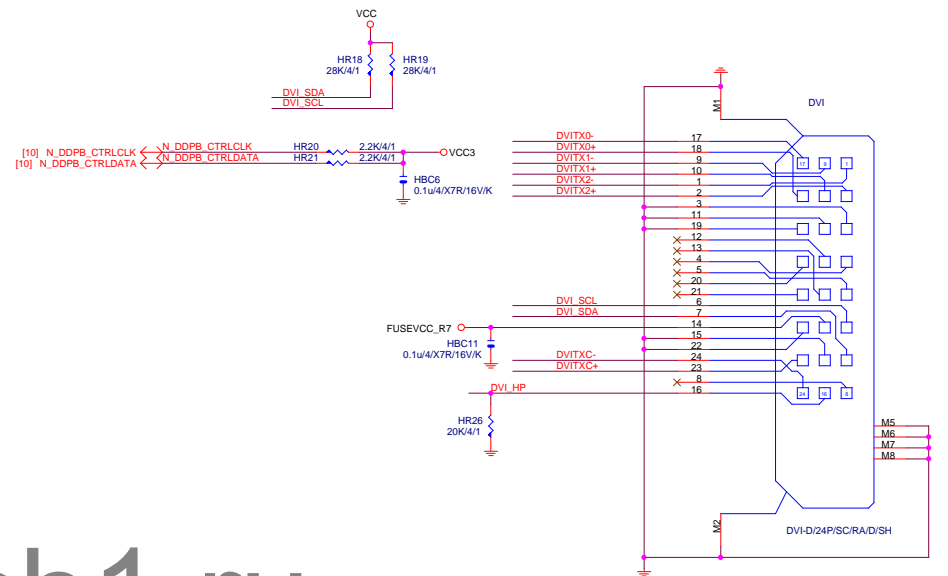
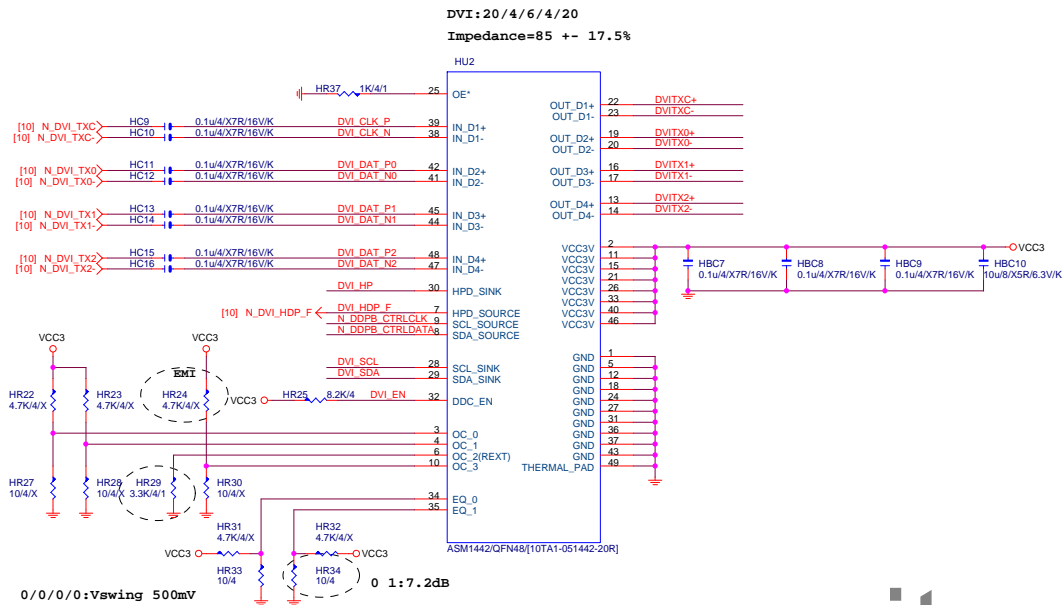


USB3.0 --> 5GHz

BANDWITH=5GHz\*(8b/10b)=4Gb/s=500MB/s

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Title E-TRON EJ168		
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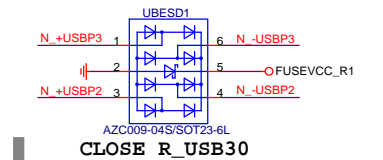
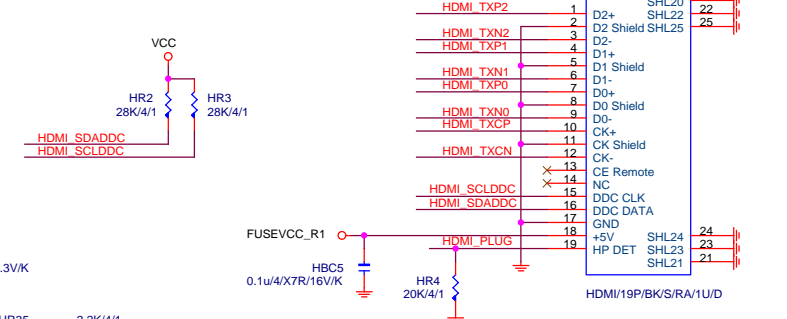
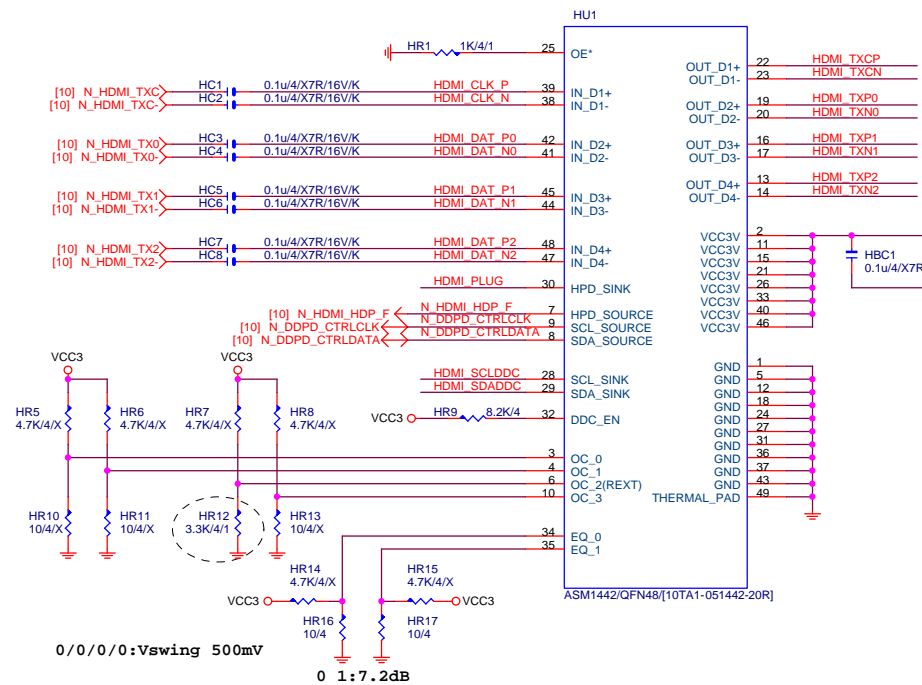




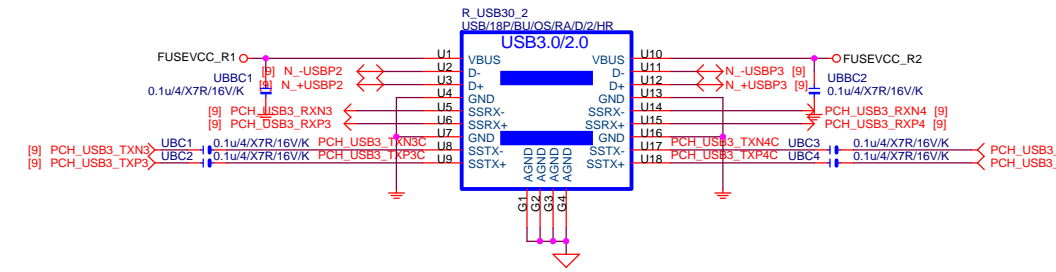
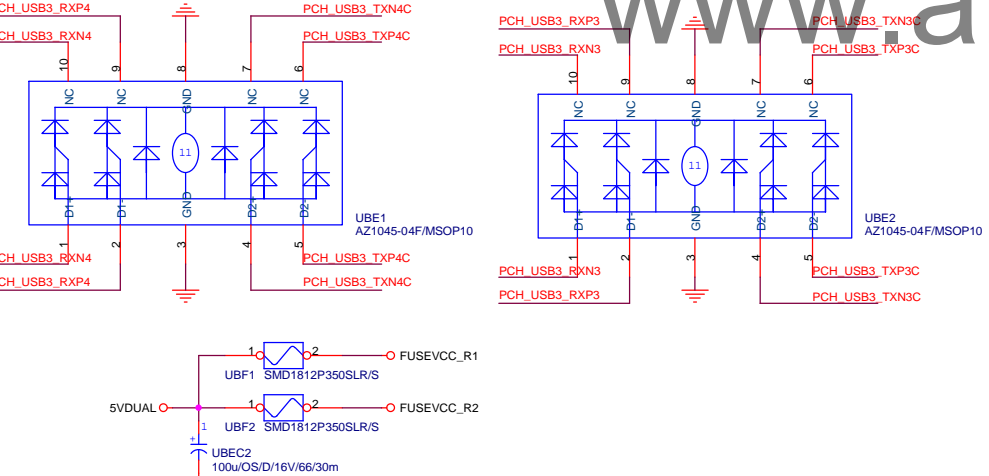
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TI TSB43AB23 1394			
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HDMI:20/4/6/4/20  
Impedance=85 +- 17.5%



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HDMI & USB			
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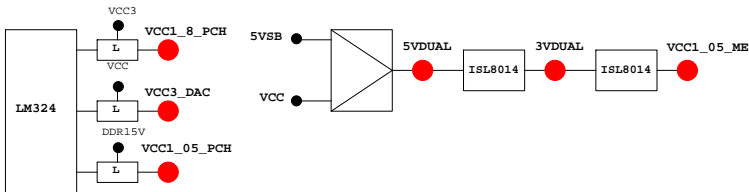
PCH GPIO LIST TABLE

PIN NAME	PWR	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI -PECI_REQ	N/A
GP1/TACH1	MAIN		GPI ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI -PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI -PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI -PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI -PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE OC5#	N/A
GP10/OC6#	STBY		NATIVE OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE -SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE OC7#	N/A
GP15	STBY	L	GPO GPIO15	N/A
GP16	MAIN		GPI -SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI -LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE -LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE -CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE -ACZ_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI GPIO29	N/A
GP30	STBY	H-Z	GPI S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI -PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI -LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI -LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE OC1#	N/A
GP41	STBY		NATIVE OC2#	N/A
GP42	STBY		NATIVE OC3#	N/A
GP43	STBY		NATIVE OC4#	N/A
GP44	STBY	L	NATIVE N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE -LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE PSI_LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE -REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE -GNT1	N/A
GP52	MAIN		NATIVE -REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE -GNT2	N/A
GP54	MAIN		NATIVE -REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE -GNT3	N/A
GP56	STBY		NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE -SUSTAT	N/A
GP62	STBY	L	NATIVE SUSCLK	N/A
GP63	STBY	L	NATIVE GPIO63	N/A
GP64	MAIN	L	NATIVE CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE 1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE 1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL

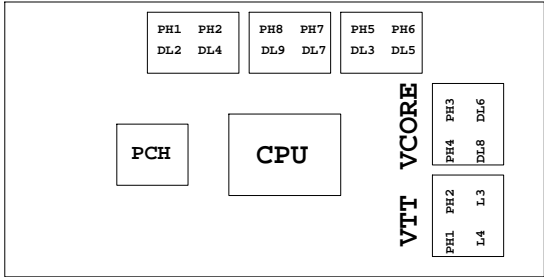
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSSO0	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSS11	SB_LED1_C	
PD4/GP74/BUSS12	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSS10	NB_LED3_C	
GP22/SCX	LOW_PWR_1	
VID05/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PWRST1	
PCIRST1#/GP12	-PFMRST2	
3VSB SW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMBC_R	2V PIN	FST_2X8
INIT#/GP85/SMBC_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#/GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBC_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXL/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VID06/GP17/RI2#	1_1V_PH_EN	
VID07/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號：

8IBP:  
1.12SP2-01A001-Y1R/Y2R  
2.12SP2-01A001-Z1R/Z2R  
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
File	TABLE LIST		
Size	Document Number	GA-Z77-D3H	
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